EECS150 - Digital Design
Lecture 19 – Review 2

April 1, 2003
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Outline

• Announcements/reminders
• List of exam topics
• Detailed discussion of quizzes and homework assignments

Please ask questions throughout!
Announcements/Reminders

• Exam 2 this Friday 4/4, 5pm, 1 Pimentel
  – ~90 minutes of relatively short questions covering the full range of topics from lectures 10-18.
  – Closed book and notes
  – Homework and quiz problems are typical
  – Similar in style and format as Exam 1
• Posted:
  – Quiz solutions, homework solutions
  – These notes
  – Exam 2 from last semester
• TA exam review this Thursday, 8pm, Room TBA

Lecture 10

General model of digital systems comprising flip-flops and combinational logic.

Determination of maximum clock frequency given characteristic delays of sub-components.

The qualitative analysis of CMOS circuits as RC circuits. The origin of gate delay. Factors effecting gate delay, both inside a gate and at the logic circuit level.

Qualitative wire delay modeling.

Origin of delays associated with flip-flops.
Lecture 11

Basics of local area networks, and structure of Ethernet frames.

Principles behind network protocol stacks.

Structure of standard hardware network-interface.

*This material will not be emphasized on the exam. However, put some thought into how to design a circuit for receiving, parsing, and filtering packets from a PHY level network interface.*

Lecture 12

Basic principles of digital video:
- progressive and interlaced scanning, horizontal and vertical blanking, and RGB versus YCbYCr pixel representation.

Principle of chroma subsampling and details of 4:2:2 and 4:2:0 schemes.

General technique for ITU601 compatible video stream generation.

Principle of frame buffer design and operation.

*The topics in this lecture should have taken on much more meaning for you now, given your experience in the lab. Although this material will not be emphasized on the exam, I will expect that you understand how to design a circuit for sending video to the encoder and understand what is needed to design a frame buffer.*
**Lecture 13**

Carry ripple adder design.

Technique for converting adder to add/sub circuit.

Carry-select addition technique.

Carry-lookahead addition technique.

Bit-serial addition.

Cost/performance analysis of ripple, carry-select, carry-lookahead, and bit-serial adders.

General familiarity with fast-carry logic in FPGAs.

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**Lecture 14**

Fundamentals of hardware multiplication.

Shift-and-Add multiplier data-path and control.

Modifications to multiplication technique for 2's-complement numbers.

Structure of array (combinational) multipliers.

Carry-save addition.

Wallace-tree multiplier.
Lecture 15

Fire Drills!

Lecture 16

Standard internal memory organization and operation.
Details of using column muxes to control aspect ratio of cell array.

Cascading memory modules to make wider or deeper memories.

Types of memories (DRAM, ROM, ...), Characteristics of S- versus DRAM.

Interface, operation, and internal organization of multi-ported memories.

Specification of memories in Verilog.

Virtex LUTs as memory blocks. Details of Virtex BlockRAMs.

Relationship between combinational logic and memory blocks.
Using ROM to implement combinational logic.
Structure and use of PLA and PLD.
Lecture 17
Details of reading and writing SDRAM.
Principles behind and details in design of FIFO memory.

Lecture 18
Design and operation of bit-serial multiplier.
Using counters with FSMs for controller implementation.
Toggle flip-flop function and design.
Structure of ripple counters.
Design of binary counters. Modification to increase max clock frequency.
Design of up/down counters.
Techniques for counting to non-power of 2 value.
Design of ring counters.