Exam III

Name: ___________________________________________________  
ID number: _____________________________________________  

This is a closed-book, closed-note exam. No calculators please. You have 2 1/2 hours. Each question is marked with its number of points (one point per expected minute of time).

Put your name and SID on each page. You can work out your answers on the backs of the pages and use the extra blank sheets at the end of the booklet. Show your work. Write neatly and be well organized. Good luck!

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1. [10pt]

a) Draw in the output waveform for the asynchronous SR latch.

b) Draw in the output waveform for the positive edge-triggered JK flip-flop.

c) Sketch a circuit diagram for a level sensitive D-type latch using only an asynchronous SR latch and simple logic gates:
d) Sketch a circuit diagram for a positive edge-triggered SR flip-flop using only an asynchronous SR latch, a level sensitive D-type latch, and simple logic gates.
2. One block of a CMOS integrated circuit is made up of 100,000 logic gates, each with average output switching energy of 10 pJoule (10 x 10^{-12} Joule). Through the course of a particular computational task, every gate switches its output on each clock cycle with probability equal to 0.1.

a) With a 100MHz clock frequency, what is the total average power consumption for the block? (Show your work)

b) Assuming the computational task takes 2 seconds to execute, what is the total energy consumption?

c) With a 5volt power supply, what would be the average measured current consumed by the block?

d) If we reduce the clock frequency to 50MHz without changing any other of the circuit parameters, what now is the total energy consumption for the same computational task?
3. [12pt] Consider a Mealy style finite state machine with the following state transition diagram. It has a single input, IN, and a single output, OUT.

   a) Draw the circuit diagram for the machine:

   b) Draw the state transition diagram for a Moore style finite state machine with the same behavior:

   c) Draw the circuit diagram for the Moore machine:
4. Imagine a datapath that has four computation units, $\alpha$, $\beta$, $\Phi$, and $\lambda$. Each computation unit requires an entire clock cycle (minus flip-flop overhead) to complete its operation. The graph below represents an iterative operation to be completed on the datapath. Each node is labeled with the name of the computation unit that it requires plus a unique integer, as a superscript. There is no feedback (or loop carry dependence) in this computation.

![Graph of iterative operation](image)

By filling in the chart below, show how to complete four iterations of the loop in the minimum number of cycles. Fill the chart using the unique integer node numbers from the graph. Use subscripts (1, 2, 3, & 4) to indicate the iteration number. For instance “32” indicates node 3 of iteration 2.

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5. [15pt] Consider the circuit shown below. On every cycle it receives a new set of inputs. On cycle number $k$ it receives a new set of inputs, $a_0^k-a_3^k$, $b_0^k-b_3^k$, and $c_0^k-c_3^k$.

a) Add flip-flops to the circuit to maximize its throughput. Indicate the addition of a flip-flop on a wire by crossing the wire with a dashed line as follows:

On each cycle, the modified circuit must accept a complete set of inputs, $a_0^k-a_3^k$, $b_0^k-b_3^k$, and $c_0^k-c_3^k$ and produce a set of outputs, $x_0^j-x_3^j$ (the value of the superscript $k$ need not equal the value of $j$). Please try out your solution on scrap paper before transferring it to the circuit above.
b) In terms of clock cycles, what is the ratio of the latency of your solution to the original circuit?

c) In terms of clock cycles, what is the ratio of the throughput of your solution to the original circuit?

d) Ignoring flip-flop delay, and assuming that the AND-gate delay is the same as the OR-gate delay, what is the ratio of the clock period for your solution to that of the original circuit?

d) Now assume that the inputs come bit-serially as follows:
   cycle 1: \( a_0^0, b_0^0, \) and \( c_0^0, \)
   cycle 2: \( a_1^0, b_1^0, \) and \( c_1^0, \)
   cycle 3: \( a_2^0, b_2^0, \) and \( c_2^0, \)
   cycle 4: \( a_3^0, b_3^0, \) and \( c_3^0, \)
   cycle 5: \( a_0^1, b_0^1, \) and \( c_0^1, \)
   cycle 6: \( a_1^1, b_1^1, \) and \( c_1^1, \) etc.

Draw a circuit that generates one bit of the result per cycle and minimizes the cost. Label and describe the operation of any control signals you may need to add.
6. [8pt] A LFSR circuit produces the following output sequence:

..., 1110, 0101, 1010, 1101, 0011, 0110, 1100, 0001, 0010, 0100, 1000, 1001, 1011, 1111, 0111, ...

a) Write down its generating polynomial expression:

b) Draw the circuit (ignore reset and initialization):
7. [10pt] A memory system uses a single error correcting Hamming code to protect its contents against errors. A word is read from memory with the following bit pattern:

011111001001

Assuming a single error occurred, what bit pattern was written to memory? Show your work.
8. [10pt] Consider the design of a simple processor whose task is to add up the absolute values of the contents of the first 100 memory locations in a memory, leaving the final result in the register labeled Z. The first 100 memory locations in memory hold 2’s complement integers. The datapath for the processor is shown below. As drawn, it has 9 control signals: the load enable and reset signal for each of the four registers, and the subtract control for the adder/subtractor circuit. The adder/subtractor circuit subtracts its right-hand input from its left-hand when sub=1. When sub=0, it adds it two inputs. The memory module has asynchronous read.

The datapath as drawn is missing some circuitry needed to complete the task.
a) Assume that the controller (not shown) is a simple finite state machine with fewer than 32 states. Neatly, modify the circuit diagram by drawing in any extra circuitry needed to complete the task and to interface the datapath to the controller. Clearly label any extra control signals that you add in. You do not need to design or show the controller circuit. 

(Simplicity counts! Try to make your additions as simple as possible.)

b) Based on your completed datapath, write the RTL description for the task.