1. Problems from Mano's book:

10-13.

(a) Four-input NAND CMOS gate

(b) Four-input NOR CMOS gate

10-16. A master-slave D FF using transmission gates and inverters.

2.

a) 3-input NAND gate

b) \( Y = (A(B+C))' \)
c) 2-input NAND-gate with tri-state output

![NAND-gate diagram]

3.

a) The circuit functions as a tri-state buffer:

![Tri-state buffer diagram]

b) \( F = a + b \cdot c + d \)

c) \( F = a \oplus b \)

4.

a) 

![Waveform diagram]

b) \( X \) functions as a **synchronous reset** signal, because it resets the output to zero when it is asserted at the active edge of the clock.
Notice that, since the first bit is sent to the output in the same cycle when LD is asserted, there is no need to store this first bit in a flip-flop.