Transistor-level Flip-flop Circuit

Positive Level-sensitive latch:

Latch Transistor Level:

Positive Edge-triggered flip-flop built from two level-sensitive latches:
General Model of Synchronous Circuit

• How do we measure performance?
  – operations/sec?
  – cycles/sec?
• What limits the clock rate?
• What happens as we increase the clock rate?

Limitations on Clock Rate

1 Logic Gate Delay

2 Delays in flip-flops

• What are typical delay values?
• Both times contribute to limiting the clock period.

• What must happen in one clock cycle for correct operation?
• Assuming perfect clock distribution (all flip-flops see the clock at the same time):
  – All signals connected to FF inputs must be ready and “setup” before rising edge of clock.

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**Example**

- Parallel to serial converter:

```
+----------------+   +----------------+
|     FF         |   |     FF         |
|  clk→Q        |   |  clk→Q        |
+----------------+   +----------------+
```

- \( T \geq \text{time}(\text{clk→Q}) + \text{time}(\text{mux}) + \text{time(\text{setup})} \)
- \( T \geq \tau_{\text{clk→Q}} + \tau_{\text{mux}} + \tau_{\text{setup}} \)

**General Model of Synchronous Circuit**

- In general, for correct operation:
  \[
  T \geq \text{time}(\text{clk→Q}) + \text{time}(\text{CL}) + \text{time(setup)}
  \]
- \( T \geq \tau_{\text{clk→Q}} + \tau_{\text{CL}} + \tau_{\text{setup}} \) for all paths.

- How do we enumerate all paths?
  - Any circuit input or register output to any register input or circuit output.
  - “setup time” for circuit outputs depends on what it connects to
  - “clk-Q time” for circuit inputs depends on from where it comes.
Timing Behavior of Logic Circuits

- Improved Transistor Model: **nFET**
  - We refer to transistor "strength" as the amount of current that flows for a given \( V_{ds} \) and \( V_{gs} \).
  - The strength is linearly proportional to the ratio of \( W/L \).

- **pFET**

Gate Switching Behavior

- **Inverter:**
  - Models inputs to other gates & wire capacitance

- **NAND gate:**

• Cascaded gates:

“transfer curve” for inverter.

Gate Delay

• Fan-out:

Each logic cell contributes capacitance

The delay of a gate is proportional to its output capacitance. Because, gates 2 and 3 turn on/off at a later time. (It takes longer for the output of gate 1 to reach the switching threshold of gates 2 and 3 as we add more output capacitance.)
“Critical” Path

- **Critical Path**: the path with the maximum delay, from any input to any output.
  - In general, we include register set-up and clk-to-Q times in critical path calculation.
- What is the critical path in this circuit?
- Why do we care about the critical path?

Delay in Flip-flops

- Setup time results from delay through first latch.
- Clock to Q delay results from delay through second latch.
Wire Delay

• In general, wires behave as “transmission lines”:
  – signal wave-front moves close to the speed of light
    • ~1ft/ns
  – Time from source to destination is called the “transit time”.
  – In ICs most wires are short, and the transit times are relatively short compared to the clock period and can be ignored.
  – Not so on PC boards.

Wire Delay

• Even in those cases where the transmission line effect is negligible:
  – Wires possess distributed resistance and capacitance
  – Time constant associated with distributed RC is proportional to the square of the length

• For short wires on ICs, resistance is insignificant (relative to effective R of transistors), but C is important.
  – Typically around half of C of gate load is in the wires.

• For long wires on ICs:
  – busses, clock lines, global control signal, etc.
  – Resistance is significant, therefore distributed RC effect dominates.
  – signals are typically “rebuffered” to reduce delay:
Clock Skew

- Unequal delay in distribution of the clock signal to various parts of a circuit:
  - if not accounted for, can lead to erroneous behavior.
  - Comes about because:
    - clock wires have delay,
    - circuit is designed with a different number of clock buffers from the clock source to the various clock loads, or
    - buffers have unequal delay.
  - All synchronous circuits experience some clock skew:
    - more of an issue for high-performance designs operating with very little extra time per clock cycle.

![Clock Skew Diagram]

Clock Skew (cont.)

- If clock period \( T = T_{\text{CL}} + T_{\text{setup}} + T_{\text{clk} \rightarrow \text{Q}} \), circuit will fail.
- Therefore:
  1. Control clock skew
     - Careful clock distribution. Equalize path delay from clock source to all clock loads by controlling wires delay and buffer delay.
     - don’t “gate” clocks.
  2. \( T \geq T_{\text{CL}} + T_{\text{setup}} + T_{\text{clk} \rightarrow \text{Q}} \) + worst case skew.
- Most modern large high-performance chips (microprocessors) control end to end clock skew to a few tenths of a nanosecond.
Clock Skew (cont.)

- Note reversed buffer.
- In this case, clock skew actually provides extra time (adds to the effective clock period).
- This effect has been used to help run circuits as higher clock rates. Risky business!