EECS150 - Digital Design

Lecture 16 - Power

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Outline

• Motivation for design constraints of power consumption
• Power metrics
• Power consumption analysis in CMOS
• How can a logic designer control power?
Is Power Consumption Important?

“The internet and wireless services are getting married”, Simon Segars

Motivation

Why should a digital designer care about power consumption?

• Portable devices:
  – handhelds, laptops, phones, MP3 players, cameras, … all need to run for extended periods on small batteries without recharging
  – Devices that need regular recharging or large heavy batteries will lose out to those that don’t.

• Power consumption important even in “tethered” devices.
  – System cost tracks power consumption:
    • power supplies, distribution, heat removal
  – power conservation, environmental concerns

• In a span of 10 years we have gone from designing without concern for power consumption to (in many cases) designing with power consumption as the primary design constraint!
Battery Technology

- Battery technology has moved very slowly
  - Moore’s law does not seem to apply
- Li-Ion and NiMh still the dominate technologies
- Batteries still contribute significant to the weight of mobile devices

![Images of Nokia 61xx, Handspring PDA, Toshiba Portege 3110 laptop]

Basics

- Power supply provides energy for charging and discharging wires and transistor gates. The energy supplied is stored & then dissipated as heat.

\[ P \equiv \frac{dw}{dt} \]

**Power:** Rate of work being done w.r.t time. Rate of energy being used.

- If a differential amount of charge \(dq\) is given a differential increase in energy \(dw\), the potential of the charge is increased by: \(V = \frac{dw}{dq}\)
- By definition of current: \(I = \frac{dq}{dt}\)

\[ dw / dt = \frac{dw}{dq} \times \frac{dq}{dt} \]

\[ P = V \times I \]

A very practical formulation!

\[ w = \int_{-\infty}^{t} Pdt \]

**total energy**

If we would like to know total energy
Basics

• **Warning!** In everyday language, the term “power” is used incorrectly in place of “energy.”
• Power is *not* energy.
• Power is *not* something you can run out of.
• Power can *not* be lost or used up.
• It is *not* a thing, it is merely a rate.
• It can *not* be put into a battery any more than velocity can be put in the gas tank of a car.

Metrics

How do we measure and compare power consumption?
• One popular metric for microprocessors is: **MIPS/watt**
  – MIPS, millions of instructions per second.
    • Typical modern value?
  – Watt, standard unit of power consumption.
    • Typical value for modern processor?
  – MIPS/watt is reflective of the tradeoff between performance and power. Increasing performance requires increasing power.
  – Problem with “MIPS/watt”
    • MIPS/watt values are typically not independent of MIPS
      – techniques exist to achieve very high MIPS/watt values, but at very low absolute MIPS (used in watches)
    • Metric only relevant for comparing processors with a similar performance.
  – One solution, **MIPS²/watt**. Puts more weight on performance.
Metrics

• How does MIPS/watt relate to energy?
• Average power consumption = energy / time

MIPS/watt = instructions/sec / joules/sec = instructions/joule

– therefore an equivalent metric (reciprocal) is energy per operation (E/op)

• E/op is more general - applies to more that processors
  – also, usually more relevant, as batteries life is limited by total energy draw.
  – This metric gives us a measure to use to compare two alternative implementations of a particular function.

Power in CMOS

Switching Energy:
energy used to switch a node

Calculate energy dissipated in pullup:

\[ E_{sw} = \int_{t_0}^{t_1} P(t) dt = \int_{t_0}^{t_1} (V_{dd} - v) \cdot i(t) dt = \int_{t_0}^{t_1} (V_{dd} - v) \cdot c (dv/dt) dt = \]

\[ = cV_{dd} \int_{t_0}^{t_1} dv - c \int_{t_0}^{t_1} v \cdot dv = cV_{dd}^2 - 1/2 cV_{dd}^2 = 1/2 cV_{dd}^2 \]

Energy supplied  Energy stored  Energy dissipated

An equal amount of energy is dissipated on pulldown.
Switching Power

• Gate power consumption:
  - Assume a gate output is switching its output at a rate of:
    \[ P_{\text{avg}} = E / \Delta t = \text{switching rate} \cdot E_{\text{sw}} \]
    
    Therefore:
    \[ P_{\text{avg}} = \alpha \cdot f \cdot 1/2 cV_{dd}^2 \]

• Chip/circuit power consumption:
  \[ P_{\text{avg}} = n \cdot \alpha_{\text{avg}} \cdot f \cdot 1/2 c_{\text{avg}} V_{dd}^2 \]

Other Sources of Energy Consumption

• “Short Circuit” Current:
  10-20% of total chip power

• Junction Diode Leakage:
  1 nWatt/gate
  few mWatts/chip

Transistor drain regions “leak” charge to substrate.
Other Sources of Energy Consumption

- Consumption caused by “DC leakage current” (Ids leakage):

\[ \text{Ids} = \frac{I_{\text{off}}}{V_{\text{out}}=V_{\text{dd}}} \]

Transistor's drain conductance never turns off all the way.

Low voltage processes much worse.

- This source of power consumption is becoming increasingly significant as process technology scales down.
- For 90nm chips around 10-20% of total power consumption. Estimates put it at up to 50% for 65nm.

Controlling Energy Consumption

What control do you have as a designer?

- Largest contributing component to CMOS power consumption is switching power:

\[ P_{\text{avg}} = n \cdot \alpha \cdot f^{1/2} \cdot c \cdot V_{dd}^2 \]

- Factors influencing power consumption:
  - \( n \): total number of nodes in circuit
  - \( \alpha \): activity factor (probability of each node switching)
  - \( f \): clock frequency (does this effect energy consumption?)
  - \( V_{dd} \): power supply voltage

- What control do you have over each factor?
- How does each factor affect the total energy?

In EECS150 design projects, we will not optimize for power consumption.