Today (1)

- EECS150 Intro.
  - Labs & Lab Lecture
  - Lab Policies
  - Computers
  - Webcast
  - Website & Newsgroup
  - Cardkeys

Today (2)

- Lab #1
  - A Quick Introduction to CAD
  - Verilog
  - Testing & Verification
  - CaLinx2
  - CAD Tool Demo
    - Project Navigator (& Synplify)
    - ModelSim

Labs & Lab Lecture (1)

- Watching the slides.
  - Projector.
  - Plasma Screen.
  - The LCD TVs (Channel 21), audio included.

- Ask Questions!
  - If anything is unclear, please ask.
  - Otherwise, the labs are impossible.

- Try to read the labs ahead of time.
Labs & Lab Lecture (2)

- Lab lecture slides are posted early on course schedule page.
- Lab ZIP file.
  - Contains verilog, bit-files, etc...
  - Also contains the lab assignment.
  - Password protected. Use login posted on white board. Personal accounts will be created later.
- The assignment.
  - Read & understand it ahead of time.
  - Do it, recording answers as needed.
  - Get checked off.

Labs & Lab Lecture (3)

- Checkoff
  - Answer any questions on the lab.
  - Prepare any requested demos.
  - Write down the number of hours spent (does not affect your grade).
  - A TA will sign off that you did the lab.
  - You must get checked off by the first 10 minutes (xx:20) of YOUR next lab. No late credit!

Labs & Lab Lecture (4)

- Solutions
  - We will discuss the solution in the lab lecture after the labs.

Lab Partners (1)

- Partners
  - Labs #1-#3 will be done alone.
  - Labs #4-#5 will be done in partners.
  - But we encourage you to work with others starting from lab #1!
Lab Partners (2)

- The project will be done in groups of 2.
  - Find a partner you trust. Start thinking about it now.
  - They must be in your lab section. You can switch, if necessary.

Lab Policies (1)

- Lab Policy Enforcement
  - Suspend your account.
    - Temporary for minor infractions.
    - Permanently for major problems, this makes it REALLY hard to pass the class.
  - Withhold your grades.
- Treat this lab with care.
  - You’ll be living here.

Lab Policies (2)

- Food & Drink
  - Nowhere near the computers.
  - You may eat at the small white tables.
  - CLEAN UP AFTER YOURSELVES!

- Trash
  - Trash goes in the white/gray bins.
  - Recycling in the blue bins.
  - CLEAN UP AFTER YOURSELVES!

Lab Policies (3)

- Computer Usage
  - No CS152 this semester. EE24 will be in here sometimes.
  - EECS150 has priority, but be courteous!

- Other Coursework
  - Feel free to work in here.
  - EECS150 has priority.
Computers (1)

- Computer Logins
  - Account forms will be handed out during your first lab.
  - Change your password once you get your forms.

Computers (2)

- Printing
  - There are 3 printers: A, B, and C.
  - Computers print to nearest printer.
  - We have a finite amount of paper, so print double sided!!!

Computers (3)

- Storage
  - U:\ is your permanent storage.
    - Available from all computers.
    - Very slow, too slow to use for temp files.
  - C:\users\<your username> is local storage.
    - **DELETED WHEN YOU LOG OFF, along with desktop and all your settings!**
    - Copy files back to U:\ drive or lose it.

Webcast

- Lab lecture will usually be “webcast,” but not live.
  - Slides will be posted in advance.
- ATTEND LAB LECTURE!
  - If you do not attend lab lecture, you will have serious problems finishing lab/project.
  - Webcast is not guaranteed.
Cardkeys

- Cardkeys are NOT ACTIVE.
  - For now TAs will let people in.
  - Cardkeys will be activated soon. We’ll let you know when.
- Cardkey responsibility.
  - Don’t open the door for people who are not in CS150.

Website & Newsgroup (1)

- The Website
  - http://www-inst.eecs.berkeley.edu/~cs150/.
  - Check it every day. We assume you’ve seen news after 48 hrs!
  - Assignments, labs, bug updates, etc.
- The Newsgroup
  - ucb.class.cs150. Staff will use Google Groups.
  - Great for posting lab and HW questions.
  - Don’t ask a question over e-mail if it’s appropriate for newsgroup. We may ignore your e-mail.

Questions

- Labs & Lab Lecture
- Lab Policies
- Computers
- Web-cast
- Cardkeys
- Website & Newsgroup
- Anything Administrative

Quick Introduction to CAD (1)

- CAD = Computer Aided Design
- What’s the point?

Source: Keutzer, EE244
Quick Introduction to CAD (2)

- CAD Tools
  - Synplify Pro.
  - Xilinx Map & PAR Tools.
  - ModelSim.

- CAD Tool Flow
  - The tools and the order in which they are applied to a given design.

Quick Introduction to CAD (3)

Xilinx Project Navigator

Synplify Pro

Verilog HDL

VHDL

Schematic Capture

Schematic

Convert to Verilog

ModelSim

Translate, Map, PAR

iMPACT

Logic Analyzer

ChipScope

Quick Introduction to CAD (4)

- Sketch on Napkin
- Sketch on Napkin

assign Out = Q ^ In;
always @(posedge Clock) begin
  if (Reset) Q <= 1'b0;
  else Q <= In;
end

Quick Introduction to CAD (5)

- Steps to build a circuit
  - Design the circuit (on paper).
  - Write Verilog in Notepad.
  - Simulate using ModelSim.
  - Fix the bugs.
  - Re-simulate using ModelSim.
  - Synthesize.
  - Program the board and cross your fingers.
Verilog (1)

- What’s an HDL?
  - Textual description of a circuit.
  - Human and machine readable.
  - Hierarchical.
  - Meaningful naming.
- NOT A PROGRAM
  - Describe what the circuit IS.
  - Not what it DOES.

Verilog (2)

Digital Design Productivity, in Gates/Week

Source: DataQuest

<table>
<thead>
<tr>
<th>HDL Type</th>
<th>Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>Behavioral HDL</td>
<td>2K-10K</td>
</tr>
<tr>
<td>RTL HDL</td>
<td>1K-2K</td>
</tr>
<tr>
<td>Gates</td>
<td>100-200</td>
</tr>
<tr>
<td>Transistors</td>
<td>10-20</td>
</tr>
</tbody>
</table>

Testing & Verification (1)

- Develop a “Testbench”
  - A non-synthesized simple verilog module.
  - Drive inputs.
    - Random Test Vectors.
    - Targeted Test Vectors - Preferred.
  - Check outputs.
- Coverage is Key!
  - How many potential problems were tested?

Testing & Verification (2)

*Circuit Under Test

Test Bench generates inputs

Test Bench observes outputs
prints text messages
Testing & Verification (3)
- ModelSim does “Functional Simulation”.
  - Great for debugging!
  - Does not account for timing.
- Xilinx PAR Tools Know More.
  - After place and route, can extract timing.
  - It is possible to feed timing into ModelSim.
  - This produces a very accurate simulation.
  - Great for checking reliability and efficiency.

Testing & Verification (4)
- Hardware Verification
  - A long slow process.
  - We prefer careful simulation earlier on.
  - Bugs found here cost MILLIONS to fix.
- We skip this.
  - Does it LOOK like it works properly?
  - Close enough…

A Little Advice
- Do the Prelab.
  - Read the online tool tutorials.
  - Otherwise this lab is very long.
- Take this lab seriously.
  - We know its long and boring.
  - You’ll need to know all this by heart to pass this class with your sanity intact.

CaLinx2 Board
- Power Switch
- LEDs
- SW10
- SW9
- FPGA
- Must be OFF
- Indicates Connection
Using the CAD Tools

- Read the Tutorials.
  - [http://inst.eecs.berkeley.edu/~cs150/sp06/Documents.php](http://inst.eecs.berkeley.edu/~cs150/sp06/Documents.php)
  - There are tutorials on EVERY CAD TOOL YOU NEED.

- Manage Your Files.
  - Remember to copy back to U:\.
  - Clean Xilinx projects before saving.

- Please ask questions.