Digital Video

EECS150 Spring 2006 – Lab Lecture #7
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Today

- Digital Video
- Administrative Info
- ITU-R BT.601
- ITU-R BT.656
- Video Encoder
- I^2C Bus
- More Information
Digital Video (1)

- **Pixel Array**
  - A digital image is represented by a matrix of pixels which include color information.

- **Frames**
  - Motion is created by flashing a series of still frames
Scanning

- Images are generated on the screen by scanning pixel lines, left to right, top to bottom.
- Early CRTs required time to get from the end of a line to the beginning of the next. Therefore each line of video consists of active video portion and a horizontal blanking interval. Even more time is needed for the CRT gun to transition from the end of the last line to the start of the first, requiring each frame to have a vertical blanking interval.
- To reduce flicker, each frame is divided into two fields: odd and even.
Colors

- Usually represented as red, green and blue
  - In the digital domain we could transmit 8 bits for each RGB component.

Transition from Black & White

- Kept compatible with old TV sets
- Added separate color or “Chroma” signals
  - Y: Luma (Traditional Black and White)
  - Cr: Chroma Red (New color signal)
  - Cb: Chroma Blue (New color signal)
Digital Video (4)

- Digital Chroma Subsampling
  - Human eye is more sensitive to Luma than Chroma; use this to save space and bandwidth

```
  RGB 4:4:4   Y  C_R  C_B  4:4:4   4:2:2 (ITU-601)   4:2:0 (MPEG-1)   4:2:0 (MPEG-2)
  R_0  R_1   Y_0  Y_1   Y_0  Y_1   Y_0  Y_1   Y_0  Y_1
  R_2  R_3   Y_2  Y_3   Y_2  Y_3   Y_2  Y_3   Y_2  Y_3
  G_0  G_1   C_B  C_B   C_B 0-1   C_B 0-3   C_B 0-3
  G_2  G_3   C_B  C_B   C_B 2-3
  B_0  B_1   C_R  C_R   C_R 0-1   C_R 0-3   C_R 0-3
  B_2  B_3   C_R  C_R   C_R 0-1
```
Administrative Info (1)

- **Design Review Process**
  - Walk your lab TA through the module
    - Control/Datapath
    - Top-down design with interconnections
  - Errors will be pointed out, but corrections are left up to you
  - Ideal duration: 10 minutes
  - It’s a team effort!
- Convince us you know what you’re doing!
ITU-R BT.601

- Formerly, CCIR-601.
  - Designed for digitizing broadcast NTSC
    - America’s National Television System Committee
- Variations:
  - 4:2:0 Chroma Subsampling
  - PAL (European) version
- Component streaming:
  - line i: $C_B \ Y \ C_R \ Y \ C_B \ Y \ C_R \ Y$
  - line i+1: $C_B \ Y \ C_R \ Y \ C_B \ Y \ C_R \ Y$
- Effective Bits/Pixel:
  - 4 components / 2 pixels = $32/2 = 16$ bits/pixel

<table>
<thead>
<tr>
<th>Active Frame Size</th>
<th>720 x 507</th>
</tr>
</thead>
<tbody>
<tr>
<td>Frame Rate</td>
<td>29.97 / sec</td>
</tr>
<tr>
<td>Scan</td>
<td>Interlaced</td>
</tr>
<tr>
<td>Chroma subsampling</td>
<td>4:2:2</td>
</tr>
<tr>
<td></td>
<td>2:1 in X only Coincident</td>
</tr>
<tr>
<td>Bits per component</td>
<td>8</td>
</tr>
<tr>
<td>Effective bits/ pixel</td>
<td>16</td>
</tr>
</tbody>
</table>
ITU-R
BT.656 (1)

- **Details**
  - Pixels/Line: 858
  - Lines/Frame: 525
  - Frames/S: 29.97
  - Pixels/S: 13.5M

- **Active**
  - Pixels/Line: 720
  - Lines/Frame: 507

- **Blanking**
  - SAV/EAV: 4B/4B
  - Black filler

**Note 1** – Sample identification numbers in parentheses are for 625-line systems where these differ from those for 525-line systems. (See also Recommendation ITU-R BT.803.)
ITU-R BT.656 (2)

- **Odd Field (262 Lines)**
  - Total: 262 Lines
  - 6 Vertical Blanking
  - 254 Active
  - 2 Vertical Blanking

- **Even Field (263 Lines)**
  - Total: 263 Lines
  - 7 Vertical Blanking
  - 253 Active
  - 3 Vertical Blanking
ITU-R BT.656 (3)

<table>
<thead>
<tr>
<th>P9</th>
<th>P8</th>
<th>P7</th>
<th>P6</th>
<th>P5</th>
<th>P4</th>
<th>P3</th>
<th>P2</th>
</tr>
</thead>
<tbody>
<tr>
<td>1'b1</td>
<td>1'b1</td>
<td>1'b1</td>
<td>1'b1</td>
<td>1'b1</td>
<td>1'b1</td>
<td>1'b1</td>
<td></td>
</tr>
<tr>
<td>1'b0</td>
<td>1'b0</td>
<td>1'b0</td>
<td>1'b0</td>
<td>1'b0</td>
<td>1'b0</td>
<td>1'b0</td>
<td></td>
</tr>
<tr>
<td>1'b0</td>
<td>1'b0</td>
<td>1'b0</td>
<td>1'b0</td>
<td>1'b0</td>
<td>1'b0</td>
<td>1'b0</td>
<td></td>
</tr>
</tbody>
</table>

**SAV Header**

- **F**: Field Select (0: Odd, 1: Even)
- **V**: Vertical Blanking Flag
- **H**: EAV/SAV Flag (0: SAV, 1: EAV)
Video Encoder (1)

- Analog Devices ADV7194
  - Supports ITU-R BT.601/656
  - S-Video and Composite Outputs
  - I²C Control (We will give this to you)
### Video Encoder (2)

<table>
<thead>
<tr>
<th>Signal</th>
<th>Width</th>
<th>Dir</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>VE_P</td>
<td>10</td>
<td>O</td>
<td>Outoing NTSC Video (Use {Data, 2’b00})</td>
</tr>
<tr>
<td>VE_SCLK</td>
<td>1</td>
<td>O</td>
<td>I^2C Clock (For Initialization)</td>
</tr>
<tr>
<td>VE_SDA</td>
<td>1</td>
<td>O</td>
<td>I^2C Data (For Initialization)</td>
</tr>
<tr>
<td>VE_PAL_NTSC</td>
<td>1</td>
<td>O</td>
<td>PAL/NTSC Mode Select (Always 1’b0)</td>
</tr>
<tr>
<td>VE_RESET_B</td>
<td>1</td>
<td>O</td>
<td>Active low reset (~Reset)</td>
</tr>
<tr>
<td>VE_HSYNC_B</td>
<td>1</td>
<td>O</td>
<td>Manual Control (Always 1’b1)</td>
</tr>
<tr>
<td>VE_VSYNC_B</td>
<td>1</td>
<td>O</td>
<td>Manual Control (Always 1’b1)</td>
</tr>
<tr>
<td>VE_BLANK_B</td>
<td>1</td>
<td>O</td>
<td>Manual Control (Always 1’b1)</td>
</tr>
<tr>
<td>VE_SCRESET</td>
<td>1</td>
<td>O</td>
<td>Manual Control (Always 1’b0)</td>
</tr>
<tr>
<td>VE_CLKIN</td>
<td>1</td>
<td>O</td>
<td>Clock (27MHz, Just send Clock)</td>
</tr>
</tbody>
</table>
**Video Encoder (3)**

<table>
<thead>
<tr>
<th>Signal</th>
<th>Width</th>
<th>Dir</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Clock</td>
<td>1</td>
<td>I</td>
<td>Clock input (27MHz)</td>
</tr>
<tr>
<td>Reset</td>
<td>1</td>
<td>I</td>
<td>Reset input</td>
</tr>
<tr>
<td>DI[n]</td>
<td>32</td>
<td>I</td>
<td>Requested Data from ROM</td>
</tr>
<tr>
<td>InRequest</td>
<td>1</td>
<td>O</td>
<td>Request Data from ROM</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>DI[n] will be valid after rising edge</td>
</tr>
<tr>
<td>InRequestLine</td>
<td>9</td>
<td>O</td>
<td>Line of Video ({Line[7:0], Field})</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>The ROM will return a pixel from this line</td>
</tr>
<tr>
<td>InRequestPair</td>
<td>9</td>
<td>O</td>
<td>Pair of Pixels</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>The line will return data for this pixel pair</td>
</tr>
</tbody>
</table>
Video Encoder (4)

General Video Encoder Block Diagram

- **Test ROM**
- **32b NTSC Video (No Blank) Address**
- **Video Line & Pair**
- **H Count**
- **V Count**
- **H FSM**
- **V FSM**
- **3.5b Clipped YC'YCb (0x10: Data, 0xF0)**
- **Data Clip**
- **Blank Gen (Mux)**
- **I2C Clock & Data**
- **I2C Done**
- **Outgoing Video (S-Video Out Cable)**
- **10b NTSC Video (Complete)**
- **Monitor**
- **ADV7194**
Video Encoder (5)

- **Basic Design**
  - Stream EAV, Blank, SAV, Active Lines
    - Generate EAV/SAV/Blank using a multiplexer
    - Register output data (Timing reasons)
  - Request Incoming Data
    - Request it the cycle before you need it
    - Clipping data
      - Minimum data is 0x10
      - Maximum data is 0xF0
      - Otherwise it will appear to be blanking signals
Video Encoder (6)

Testing

- Test thoroughly
  - Simulation is difficult with test ROM
  - Try using values which count, so you can see it

- Design your testbench early
  - Perhaps one partner should design the module, one should design the testbench
  - Ensure that you test corner cases
    - First and last lines
    - Off-by-one errors in counters
I\textsuperscript{2}C (1)

- ADV7194 Initialization using I\textsuperscript{2}C
  - Requires only 2 wires
    - Serial Data (Bidirectional)
    - Clock (Driven by master)
  - Runs at up to 400kHz
  - Bidirectional Communication
- Given to you
  - Complicated to get right
  - Hard to debug
I\(^2\)C (2)

- Physical Protocol
  - Data
    - Open collector bidirectional bus
    - Driven by sender
  - Clock
    - Open collector unidirectional bus
    - Driven by master
    - May be pulled low to stall transmission

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Bidirectional Open Collector Bus

Endpoint A

- Din
- Enable
- DOut

10kΩ Pullup

Endpoint B

- Din
- Enable
- DOut

10kΩ Pullup
I²C (3)

- Protocol
  - Start Condition
  - Address
  - Address Acknowledge
  - Data Transfer
  - Data Acknowledge
  - Stop Condition
I^2C (4)

- Arbitration
  - Anyone can drive bus at any time
    - No central arbiter
    - No short circuits (Impossible in open collector)
  - Decentralized Arbitration
    - Check data bus against value you’re sending
    - Mismatch means someone else is transmitting
      - So let them finish, and then try again
    - Inherently gives preferences to accesses with more 1’s in them
More Information

- Checkpoint Writeup
- Documents Page of the Website
  - Video in a Nutshell
  - ADV7194 Datasheet
    - Complete ADV7194 reference
  - ITU-R BT.656 & ITU-R BT.601 Standards
    - Complete video standards
  - I²C Bus Specification

- READ THE DATASHEETS!