Digital Design and System Implementation

- Overview of Physical Implementations
- CMOS devices
- CMOS transistor circuit functional behavior
  - Basic logic gates
  - Transmission gates
  - Tri-state buffers
  - Flip-flops vs. latches revisited

Overview of Physical Implementations

The stuff out of which we make systems

- Integrated Circuits (ICs)
  - Combinational logic circuits, memory elements, analog interfaces
- Printed Circuits (PC) boards
  - Substrate for ICs and interconnection, distribution of CLK, Vdd, and GND signals, heat dissipation
- Power Supplies
  - Converts line AC voltage to regulated DC low voltage levels
- Chassis (rack, card case, ...)
- 1-25 conductive layers
  - Holds boards, power supply, fans, provides physical interface to user or other systems
- Connectors and Cables
### Integrated Circuits

- Primarily Crystalline Silicon
- 1mm - 25mm on a side
- 200 - 400M effective transistors
- (50 - 75M “logic gates”)
- 3 - 10 conductive layers
- 2007 feature size \( \sim 65\text{nm} = 0.065 \times 10^{-6} \text{m} \)
- 45nm coming on line
- “CMOS” most common - complementary metal oxide semiconductor

**Package provides:**
- Spreading of chip-level signal paths to board-level
- Heat dissipation.
- Ceramic or plastic with gold wires

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### Printed Circuit Boards

- Fiberglass or ceramic
- 1-20in on a side
- IC packages are soldered down

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### Multichip Modules (MCMs)

- Multiple chips directly connected to a substrate (silicon, ceramic, plastic, fiberglass) without chip packages
Integrated Circuits

- Moore's Law has fueled innovation for the last 3 decades

- "Number of transistors on a die doubles every 18 months."

- What are the consequences of Moore's law?

**Uses for Digital IC technology today:**

- **Standard microprocessors**
  - Used in desktop PCs, and embedded applications (e.g., automotive)
  - Simple system design (mostly software development)

- **Memory chips (DRAM, SRAM)**

- **Application specific ICs (ASICs)**
  - Custom designed to match particular application
  - Can be optimized for low-power, low-cost, high-performance
  - High-design cost / relatively low manufacturing cost

- **Field programmable logic devices (FPGAs, CPLDs)**
  - Customized to particular application after fabrication
  - Short time to market
  - Relatively high part cost

- **Standardized low-density components**
  - Still manufactured for compatibility with older system designs
CMOS Devices
- MOSFET (Metal Oxide Semiconductor Field Effect Transistor)

Top View

Cross Section

The gate acts like a capacitor. A high voltage on the gate attracts charge into the channel. If a voltage exists between the source and drain a current will flow. In its simplest approximation, the device acts like a switch.

Transistor-level Logic Circuits
- Inverter (NOT gate):
- NAND gate

How about AND gate?

Note:
- out = 0 iff both a AND b = 1 therefore out = (ab)
- pFET network and nFET network are duals of one another.
Transistor-level Logic Circuits

Simple rule for wiring up MOSFETs:

- nFET is used only to pass logic zero
- pFet is used only to pass logic one
- For example, NAND gate:

Note: This rule is sometimes violated by expert designers under special conditions

Transistor-level Logic Circuits

- NAND gate
- NOR gate

Note:
- out = 0 iff both a OR b = 1 therefore out = (a+b)'
- Again pFET network and nFET network are duals of one another

Other more complex functions are possible. Ex: out = (a+bc)'
Logic and Layout: NAND Gate

Transmission Gate

- Transmission gates are the way to build “switches” in CMOS
- In general, both transistor types are needed:
  - nFET to pass zeros
  - pFET to pass ones
- The transmission gate is bi-directional (unlike logic gates)
- Does not directly connect to Vdd and GND, but can be combined with logic gates or buffers to simplify many logic structures
Pass-Transistor Multiplexer

- 2-to-1 multiplexer:
  \[ c = sa + s'b \]

- Switches simplify the implementation:

4-to-1 Pass-transistor Mux

- The series connection of pass-transistors in each branch effectively forms the AND of \( s_1 \) and \( s_0 \) (or their complement)

- 20 transistors
Alternative 4-to-1 Multiplexer

- This version has less delay from in to out
- Care must be taken to avoid turning on multiple paths simultaneously (shorting together the inputs)

36 Transistors

Example: Tally Circuit

N inputs: How many of these are asserted?

E.g., 1 input, 2 outputs: One, Zero
E.g., 2 inputs, 3 outputs: Two, One, Zero
N inputs, N+1 outputs: N, ..., One, Zero
Example: Tally Circuit

(a) Tally Circuit Diagram

(b) Tally Circuit Diagram (alternative view)

Example: Tally Circuit

(a) Tally Circuit Diagram

(b) Tally Circuit Diagram (alternative view)
Example: Tally Circuit

2 inputs, 3 outputs:
Two, One, Zero
Example: Tally Circuit

2 inputs, 3 outputs:
Two, One, Zero
Example: Tally Circuit

2 inputs, 3 outputs:

Two, One, Zero

(b) $I_1 = 0, I_2 = 1$

Example: Tally Circuit

2 inputs, 3 outputs:

Two, One, Zero

(c) $I_1 = 1, I_2 = 0$
Example: Tally Circuit

2 inputs, 3 outputs:
Two, One, Zero

Example: Crossbar Switch
N inputs, N outputs, N x N control signals

Note: circuit like this used inside Xilinx switching matrix
Example: Barrel Shifter

* N inputs, N outputs, N control signals

Diagram of a barrel shifter showing the connections and signals.
Example: Barrel Shifter
N inputs, N outputs, N control signals

Example: Barrel Shifter
N inputs, N outputs, N control signals

Example: Barrel Shifter
N inputs, N outputs, N control signals
Tri-state Buffers

**Tri-state Buffer:**

```
<table>
<thead>
<tr>
<th>CE</th>
<th>IN</th>
<th>OUT</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>
```

“high impedance” (output disconnected)

**Variations**

- Inverting buffer
- Inverted enable

**Transistor circuit for inverting tri-state buffer:**

“transmission gate”

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**Tri-state Buffers**

*Tri-state buffers are used when multiple circuits all connect to a common bus. Only one circuit at a time is allowed to drive the bus. All others “disconnect”.*

**Bidirectional connections:**

**Busses:**

CS 150 – Spring 2007 - Lec #26 – Digital Design
Tri-state Based Multiplexer

- **Multiplexer**

  ![](image1)
  
  If \( s=1 \) then \( c=a \) else \( c=b \)

- **Transistor Circuit for inverting multiplexer**

  ![](image2)

D-type Edge-triggered Flip-flop

- The edge of the clock is used to sample the "D" input & send it to "Q" (positive edge triggering)

  - At all other times the output \( Q \) is independent of the input \( D \) (just stores previously sampled value)
  - The input must be stable for a short time before the clock edge.

![](image3)

- \( D \)
  - \( clk \)

  ![](image4)

  - \( Q \)
    - \( clk \)
Transistor-level Logic Circuits

Positive Level-sensitive latch:

Latch Transistor Level:

Positive Edge-triggered flip-flop built from two level-sensitive latches:

State Machines in CMOS

- Two Phase Non-Overlapping Clocking
Digital Design and Implementation Summary

- **CMOS preferred implementation technology**
- **Much more than simple logic gates**
  - Transmission gate as a building block
  - Used to construct “steering logic”
  - Very efficient compact implementations of interconnection and shifting functions
- **Simple storage building blocks**
  - D-type flip flop behavior with cross-coupled inverters and two phase clocking
- **Heart of Xilinx implementation structures**