Integrated Circuits

- Primarily Crystalline Silicon
- 1mm - 25mm on a side
- 200 - 400M effective transistors
- (50 - 75M "logic gates")
- 3 - 10 conductive layers
- 2007 feature size = 65nm = 0.065 x 10^-6 m
- 45nm coming on line
- "CMOS" most common -
  complementary metal oxide semiconductor

- Package provides:
  - Spreading of chip-level signal paths to board-level
  - Heat dissipation.
  - Ceramic or plastic with gold wires

Fiberglass or ceramic
1 - 20in on a side
IC packages are soldered down

Multichip Modules (MCMs)
- Multiple chips directly connected to a substrate
  (silicon, ceramic, plastic, fiberglass) without chip packages

Moore's Law has fueled innovation for the last 3 decades

"Number of transistors on a die doubles every 18 months."

What are the consequences of Moore’s law?
**CMOS Devices**

- **MOSFET (Metal Oxide Semiconductor Field Effect Transistor)**

**Cross Section**

The gate acts like a capacitor. A high voltage on the gate attracts charge into the channel. If a voltage exists between the source and drain a current will flow. In its simplest approximation, the device acts like a switch.

**Top View**

Transistor-level Logic Circuits

- **Inverter (NOT gate):**

\[ \text{out} = \overline{\text{in}} \]

Note: This rule is sometimes violated by expert designers under special conditions.

**How about AND gate?**

In general, both transistor types are needed. Transmission gates are the way to build “switches” in CMOS.

- The transmission gate is bi-directional (unlike logic gates).

Does not directly connect to Vdd and GND, but can be combined with logic gates or buffers to simplify many logic structures.

Logic and Layout: NAND Gate
Pass-Transistor Multiplexer

- 2-to-1 multiplexer:
  \[ c = s_0 + s'_1 \]

- Switches simplify the implementation:
  \[ \begin{array}{c}
  a \quad s_1 \\
  b \quad s'_0 \\
  c \\
  \end{array} \]

Alternative 4-to-1 Multiplexer

- This version has less delay from in to out.
- Care must be taken to avoid turning on multiple paths simultaneously (shorting together the inputs).

  36 Transistors

4-to-1 Pass-transistor Mux

- The series connection of pass-transistors in each branch effectively forms the AND of \( s_1 \) and \( s_0 \) (or their complement)

- 20 transistors

Example: Tally Circuit

- \( N \) inputs: How many of these are asserted?
  - E.g., 1 input, 2 outputs: One, Zero
  - E.g., 2 inputs, 3 outputs: Two, One, Zero
  - \( N \) inputs, \( N+1 \) outputs: \( N, \ldots, One, Zero \)

Example: Tally Circuit

- Example: Tally Circuit
  - Straight through
  - Diagonal
  - One
  - Zero

Example: Tally Circuit

- Example: Tally Circuit
Example: Tally Circuit

2 inputs, 3 outputs:
Two, One, Zero

Diagram representation:

(a) \( I_1 = 0, I_2 = 0 \)

(b) \( I_1 = 0, I_2 = 1 \)

(c) \( I_1 = 1, I_2 = 0 \)
Example: Tally Circuit
2 inputs, 3 outputs:
Two, One, Zero

Example: Crossbar Switch
N inputs, N outputs, N x N control signals

Example: Barrel Shifter
N inputs, N outputs, N control signals

Note: circuit like this used inside Xilinx switching matrix

Example: Barrel Shifter
N inputs, N outputs, N control signals

Rotating Shift
Tri-state Buffers

Tri-state Buffer:

Transistor circuit for inverting tri-state buffer:

Variations

Tri-state Buffer:

"transmission gate"

Inverting buffer

Iverted enable

“high impedance”
(output disconnected)

D-type Edge-triggered Flip-flop

The edge of the clock is used to sample the "D" input & send it to "Q" (positive edge triggering)

At all other times the output Q is independent of the input D (just stores previously sampled value)

The input must be stable for a short time before the clock edge.

Transistor-level Logic Circuits

Positive Level-sensitive latch:

Latch Transistor Level:

Positive Edge-triggered flip-flop built from two level-sensitive latches:

State Machines in CMOS

Two Phase Non-Overlapping Clocking

In

1/2 Register

Combinational Logic

1/2 Register

State

P1

P2

CLCK

P1

P2
Digital Design and Implementation Summary

- CMOS preferred implementation technology
- Much more than simple logic gates
  - Transmission gate as a building block
  - Used to construct "steering logic"
  - Very efficient compact implementations of interconnection and shifting functions
- Simple storage building blocks
  - D-type flip flop behavior with cross-coupled inverters and two phase clocking
- Heart of Xilinx implementation structures