Today

- CAD Flow “Full Circle”
- ChipScope
- Administrative Info
- Lab #5: ChipScope & UART <-> CPU Adaptor
  - UART <-> CPU Adaptor
  - CPU Emulator
  - Echo.s
  - Using ChipScope
  - PreLab & Design Reviews

ChipScope & the UART <-> CPU Adaptor

EECS150 Spring 2009 - Lab Lecture #5

Chris Fletcher

Slides designed by Chris Fletcher
"Lab #5: Using ChipScope (2)" designed by Greg Gibeling
Pictures of the XUPv5 board sourced from Xilinx
ChipScope (1)
- Software based logic analyzer
  - Show results on the computer
  - Wave window!
- Put a logic analyzer right into the FPGA
  - ICON – Connects FPGA to software
  - ILA – Does the actual analysis
- Shows only changes at clock edge

ChipScope (2)

ChipScope (3)
- ChipScope vs. ModelSim
  - ModelSim
    - Software simulator
    - Testbench => Buggy \(\rightarrow\) ModelSim Results != Accurate
    - Easy to fix bugs and rerun simulation
    - Easy to look at every signal in your design
  - ChipScope
    - Reports what it sees happening on Hardware (no lies!)
    - Takes time to fix bug and rerun
    - Forces you to select signals to look at

The "It works in ModelSim but not on the FPGA..." slide
Administrative Info

- Lab 5 is a 2-person partner lab
- iSVN full steam ahead
  - Group access for project
- Lab lecture conflicts
  - No makeup quizzes (except 1:45pm)
- Check-off procedure
- Questions?

Lab #5: UART ↔ CPU Adaptor (1)

- Build a part of your project
- Learn to use ChipScope
- Learn to use an interface (UART)
  - Ready/Valid
- Build an interface + handshake
  - UART ↔ CPU Adaptor
- Build a CPU Emulator
  - ... to verify the UART ↔ CPU Adaptor

Lab #5: UART ↔ CPU Adaptor (2)
Lab #5: UART↔CPU Adaptor (3)

- What you are given
  - FPGA_TOP_ML505
    - Use for the rest of the semester
    - Keep clean and organized!
  - UART
    - Simple module
    - Understand how it works!
  - PUTTY / Serial Cables
  - Interface specifications
  - Functional requirements

Lab #5: UART↔CPU Adaptor (4)

- What you can use
  - Behavioral Verilog
  - Synplify RTL/Technology Schematics
  - FPGA Editor
  - ModelSim
  - ChipScope
  - Your ingenuity and creativity

Lab#5: ChipScope (1)

- Learning to use ChipScope
  - This is a very important part of the lab
- Lab check-off requires ChipScope analysis
- Objectives
  - Generating ICON/ILA cores (COREGen)
  - Learn to trigger on a signal
  - Learn to probe signal(s)
Lab#5: ChipScope (2)

- Steps to use ChipScope
  - Generate an ICON
  - Generate an ILA
  - Connect the ILA to the ICON
  - Synthesize, and implement your design
    - With the ILA and ICON
  - Program the XUPv5 board
  - Run the ChipScope Pro Analyzer

Lab#5: ChipScope (3)

- You will NEED ChipScope
  - Your last line of defense
  - You cannot debug a large design without it

Lab#5: PreLab (1)

- Project PreLabs
  - You get a specification
  - Your job will be to design a circuit to satisfy implementation requirements
  - Take your design extremely seriously
- Design Reviews
  - Starting next week
  - "Non-blocking" approach
Lab#5: PreLab (2)

- Project Partners and Design Reviews
  - Both partners must be present
  - Design reviews happen only during lab
- Design Review Guidelines
  - Come ready with your design
  - Be ready to answer your TA's questions
  - Each partner must be able to explain whole design
  - Design reviews will be graded

Lab#5: PreLab (3)

- Acceptable Designs
  - MUST be printed and neat
  - Microsoft Visio is highly recommended
    - (its what we use)
  - Electronic mediums are preferred over scans
- NOT Acceptable Designs
  - "On a napkin" (or XORs on toilet paper)
  - Crumpled pieces of paper
  - Crooked, messy or otherwise unreadable wiring

If we can’t follow it, we can’t grade it