University of California at Berkeley
College of Engineering
Department of Electrical Engineering and Computer Science

EECS150, Spring 2010

Homework Assignment 12: Adders and Other Design Blocks
Due April 23rd, 2pm

Homework submissions must be made via the course SVN repository. Email submissions will not be accepted! Please format your homework as plain text, or PDF, or another semi-universal format. Please do not submit Word files.
Before starting the problems below, please read sections 5.1-5.2 of DDCA.

1. Consider the bit-serial multiplier given in lecture 24, slide 5.
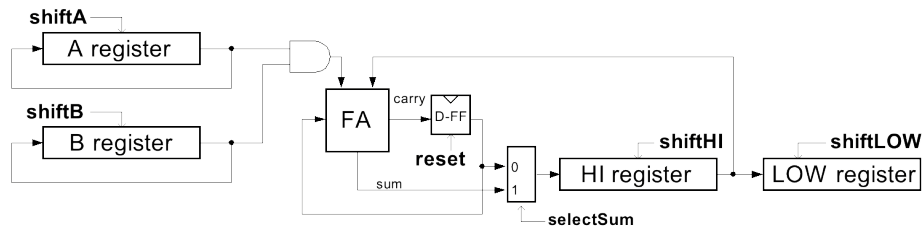
   To better understand this circuit, trace (write down the contents of registers at every cycle) the multiplication of 4'd5 by 4'b9 through a 4-bit bit-serial multiplier.

   Now propose how this multiplier can be extended to handle signed 2's complement multiplication.

2. The following are all important characteristics of any design block:

   • Latency: how many cycles does a single division take?

   • Throughput: how many divisions per cycle (a fraction) can your circuit handle? Notice that pipelining can be used to improve throughput at the cost of latency.

   • Issue rate: How often can the circuit begin a new operation? In other words, every how many cycles can the divider take a new set of inputs?

   In this problem, we will study the pop-count operator. This operator takes one 2's complement N-bit input, and produces a 2's complement output equal to the number of ones (high bits) in the input. In other words, this operator counts high bits in the input. Such an operation is useful in network interfaces to interpret data that may contain bit flips (Wikipedia 8b/10b encoding for one example). In answering the following questions, you may use gates, registers, MUXes, and N-bit adders.

   (a) Design a 16-bit combinational pop count operator. What are the latency, throughput and issue rate of this design?

(b) Design a 16-bit bit-serial pop count operator. What are the latency, throughput and issue rate of this design?

(c) In 2-3 sentences, discuss how the two designs can be combined to trade-off cost and performance.

3. The partial design of a particular 8-bit carry lookahead adder is shown below. Many details are omitted for simplicity. Not shown are the carry-in and carry-out signals, c_0 and c_8, the internal carry signals, and the output signals, $s_0 - s_7$.
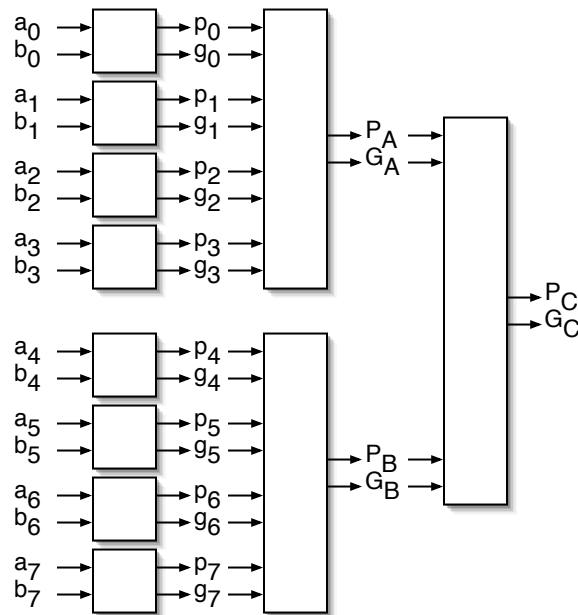
Write boolean expressions for the following signals as they would be computed in an adder with a circuit as shown above.

(a) $p_0 = $ _____

   $g_0 = $ _____

(b) $P_A = $ _____

   $G_A = $ _____

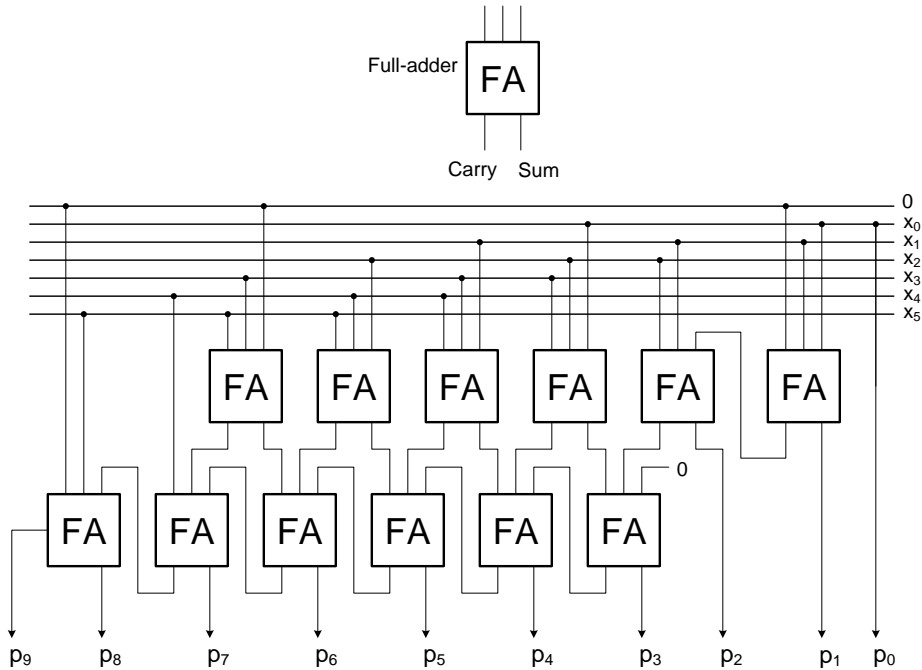(c) $P_C = $ _____

   $G_C = $ _____

(d) $c_4 = $ _____

(e) $c_8 = $ _____

(f) $s_4 =$ _____

4. (a) The circuit shown below is used to multiply the 6-bit number X by a 6-bit constant value, C. It is made up of instances of a full-adder cell. The full-adder takes as input 3 1-bit signals and outputs a 1-bit sum and a 1-bit carry.

What is the value of C?

(b) Using nothing but instances of the full-adder cell from part a), draw a circuit for adding four 3-bit numbers, $w_2w_1w_0$, $x_2x_1x_0$, $y_2y_1y_0$, and $z_2z_1z_0$. First minimize the total delay then the total number of full-adder cells. Label all inputs and outputs.

5. Consider the design of a carry-select adder using circuit elements where the delay through the 2-to-1 multiplexor (any input to output) is exactly 1/2 the delay through a full-adder cell (any input to any output): $\tau_{mux} = \frac{1}{2} \cdot \tau_{FA}$.

(a) For a 128-bit adder with all select groups the same size (s), what group size and what number of groups (g), will lead to an adder with minimal delay?

S =

g =

(b) In general, for an n-bit adder of this type (carry-select with all groups the same size), what is the optimal value for s and g as a function of n?

S =

g =

Briefly justify your answer.

6. You have a **LOT** of work to do. Please make sure you are able to finish your project.

7. **Extra for experts:**

   Bit-serial operators are interesting for a number of reasons, particularly their economy of hardware resources. Applications that impose a modest baseline throughput requirement (such as audio processing), and thus do not benefit from high-throughput arithmetic, can make excellent use of this style of design.

   Alyssa P. Hacker is wondering how to build a 16-bit bit-serial divider. Being a mighty CS150 student, propose one design for such a circuit, and compute the following for your design (if the answer is input-dependent, give the best and worst cases):

   (a) Latency
   (b) Throughput
   (c) Issue rate