University of California at Berkeley
College of Engineering
Department of Electrical Engineering and Computer Science

EECS150, Spring 2010

Homework Assignment 3: Verilog and Sequential Logic
Due February 12^{th}, 2pm

Homework submission will only be through SVN. Email submissions will not be accepted! Please format your homework as plain text with either PNG or PDF for any necessary figures. Microsoft Visio is installed on the machines in 125 Cory, and is a useful tool for drawing figures of all kinds.

1. One-hot encoding is an alternative to binary encoding. For example, in 8-bit one-hot encoding, the number 0 is represented as 00000001, the number 1 is 00000010, 2 is 00000100, 3 is 00001000, ..., 7 is 10000000. It is called "one-hot" because only 1 bit is ever on at a time. An 8-bit one-hot *counter* is a circuit whose output would count in the following sequence: 00000001, 00000010, ..., 01000000, 10000000, 00000001, ...

   Design a one-hot encoded counter. Besides the clock (clk) input, your counter should also take in as inputs a reset (rst) and an enable (en) signal. When reset is high, the counter will reset its output to 0 (00000001) at the next positive edge of the clock. If enable is high, the counter will count up to the next number in the sequence at the next positive edge of the clock. Reset has priority over enable.

   Draw a schematic diagram of your circuit and write a Verilog module that implements it.

2. Write a Verilog module for a 2:4 decoder circuit, using a) an always block, b) continuous assignment.

3. DDCA 4.19

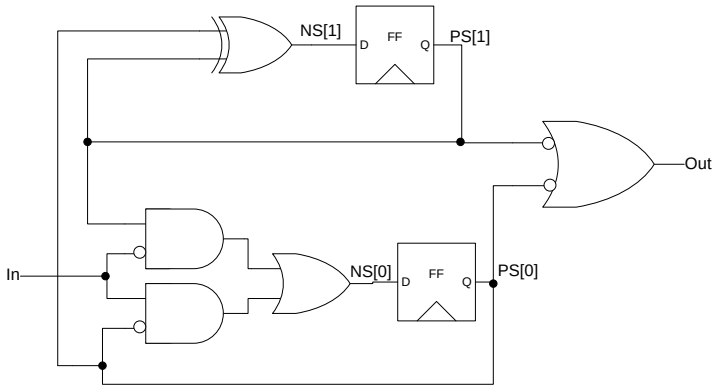
4. DDCA 4.46

5. DDCA 4.47

6. DDCA 4.48 excluding part h.

7. DDCA 4.27

8. Consider the following finite state machine (FSM) circuit:

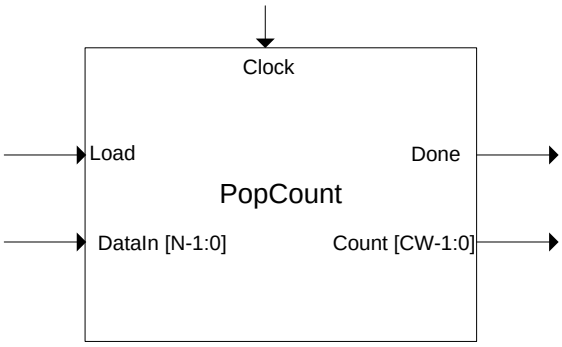


   (a) Write a Verilog description of the circuit using continuous assignment for the NS and OUT signals.

   (b) Draw a state transition diagram describing the behavior of the circuit. Within each state bubble indicate the bit encoding for that state. Remember to label the arcs with input values and state with output values.

9. A "population count" (PopCount) circuit counts the number of 1's in an N-bit signal. The interface to such a circuit is shown in the figure below. Your job is to design an N-bit wide PopCount circuit. Your implementation must count just one bit per cycle and will therefore take N cycles to complete the count. (although it is usually not optimal to design PopCount in this way).

   The Load input signal indicates a new N-bit input is available on Datain. Note that the input is loaded in parallel, not serially. The Done output signal should indicate that the count is finished (i.e. Done is high starting on the cycle when the count output becomes correct and stays high until the next time Load goes high).



   (a) If the input DataIn is N bits, how many bits must the Count output be? This is "CW" in the figure.

   (b) Draw your PopCount circuit for N=4.

   (c) Write the Verilog for the PopCount, making N a parameter.