EECS150 - Digital Design

Lecture 9- CMOS (part 2)

Feb 16, 2010

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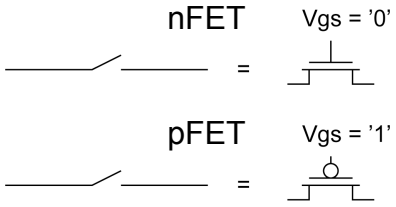
CMOS Devices

Review: Transistor switch-level models

The gate acts like a capacitor. A high voltage on the gate attracts charge into the channel. If a voltage exists between the source and drain a current will flow. In its simplest approximation, the device acts like a switch.

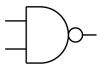


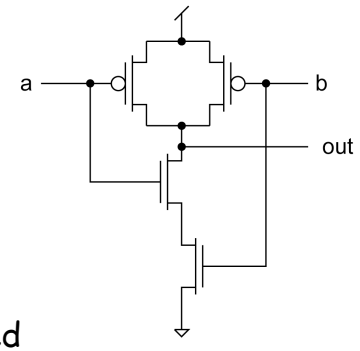
Transistor-level Logic Circuits

Simple rule for wiring up MOSFETs:

nFET is used only to pass logic zero.
pFET is used only to pass logic one.

For example, consider the NAND gate:

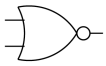


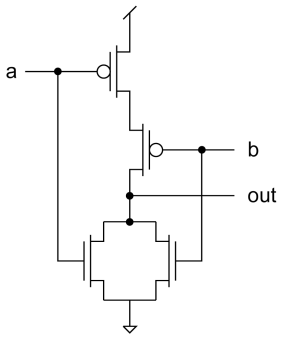


Note: This rule is sometimes violated by expert designers under special conditions.

Transistor-level Logic Circuits

NOR gate:



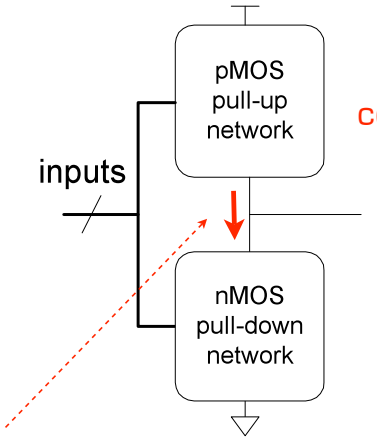


Note:

- out = 0 iff a OR b =1 therefore out = (a+b)'
- Again pFET network and nFET networks are duals of one another.

Other more complex functions are possible. Ex: out = (a+bc)'

CMOS Logic Gates in General



Pull-up network conducts under conditions to generate a logic 1 output

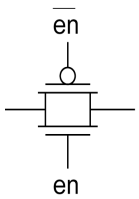
Pull-down network conducts for logic 0 output

Conductance must be mutually exclusive - else, short circuit!

Pull-up and pull-down networks are "topological duals"

Transmission Gate

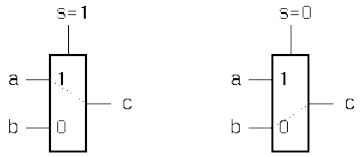
- Transmission gates are the way to build "switches" in CMOS.
- In general, both transistor types are needed:
  - nFET to pass zeros.
  - pFET to pass ones.
- The transmission gate is bi-directional (unlike logic gates).



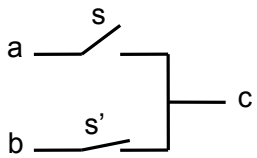
- Does not directly connect to Vdd and GND, but can be combined with logic gates or buffers to simplify many logic structures.

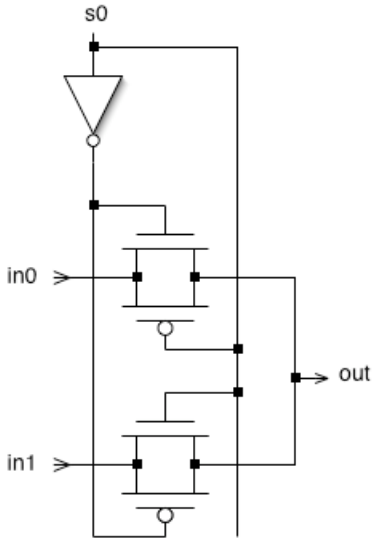
Transmission-gate Multiplexor

2-to-multiplexor:
$C = sa + s'b$



Switches simplify the implementation:

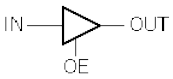




Compare the cost to logic gate implementation.

Tri-state Buffers

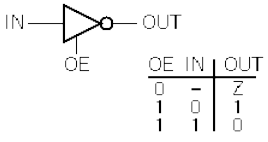
Tri-state Buffer:



OE	IN	OUT
0	0	Z
0	1	Z
1	0	0
1	1	1

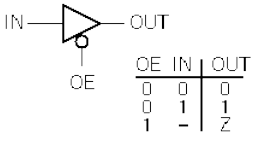
"high impedance" (output disconnected)

Variations:



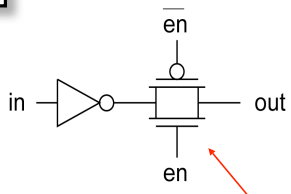
OE	IN	OUT
0	–	Z
1	0	1
1	1	0

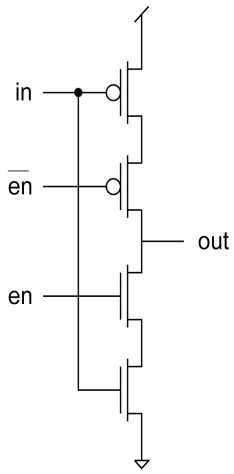
Inverting buffer



OE	IN	OUT
0	0	0
0	1	1
1	–	Z

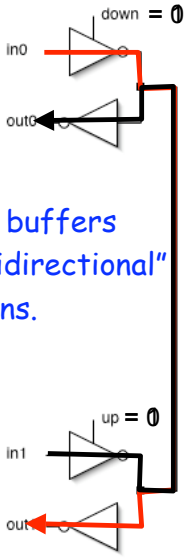
Inverted enable





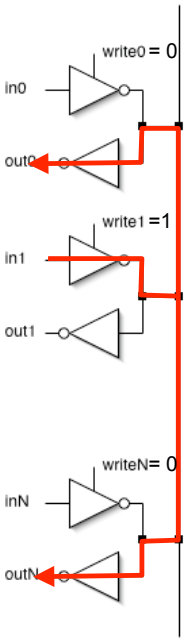
transmission gate useful in implementation

Tri-state Buffers



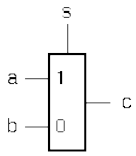
Tri-state buffers enable "bidirectional" connections.

Tri-state buffers are used when multiple circuits all connect to a common wire. Only one circuit at a time is allowed to drive the bus. All others "disconnect" their outputs, but can "listen".

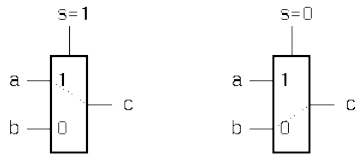


Tri-state Based Multiplexor

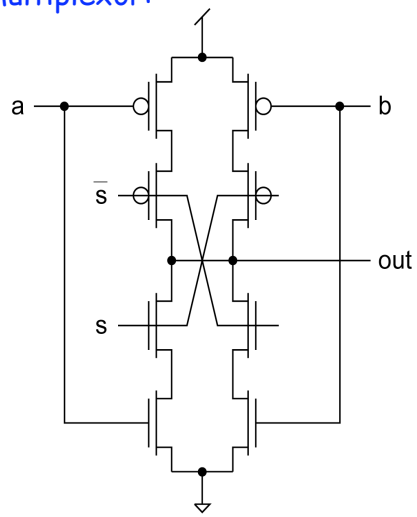
Multiplexor



If s=1 then c=a else

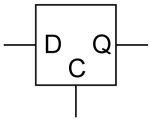


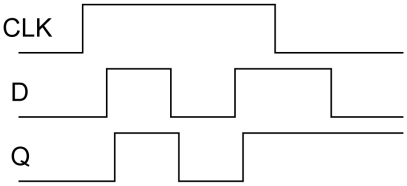
Transistor Circuit for inverting multiplexor:



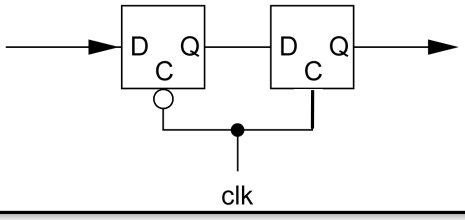
Latches and Flip-flops

Positive level-sensitive **latch**:





Positive Edge-triggered **flip-flop** built from two level-sensitive latches:



Latch Implementation: