University of California at Berkeley
College of Engineering
Department of Electrical Engineering and Computer Science

EECS150, Spring 2010

Quiz 2: February 5^{th}

In this problem, you will map the ALU BitSlice that you built in this week's lab into a simplified Virtex-5 CLB (shown in Figure 1). This CLB is composed of two ordinary Virtex-5 6LUTs and an FMUX between them. The ALU BitSlice must support the following inputs and outputs:

***a*, input, 1 bit** : The first operand.

***b*, input, 1 bit** : The second operand.

c_{in}, input, 1 bit : The carry-in.

***Result*, output, 1 bit** : The result of the operation.

c_{out}, output, 1 bit : The carry-out.

***ALUOp*, input, 3 bits** : The ALUOp.

This is exactly the same port specification as the ALU BitSlice in Lab 2. In case you don't remember, the *ALUOp* encoding from the lab is shown in Table 1. To answer the question, fill in the boxes con-

Binary Code	Operation
000	*Result* = $a + b$
001	*Result* = $a - b$
010	*Result* = a & b (bit-wise *and*)
011	*Result* = $a \mid b$ (bit-wise *or*)
100	*Result* = $a \otimes b$ (bit-wise *xor*)
101	*Result* = $\sim a$ (bit-wise *not*)
110	*Result* = a (passthrough)
111	unused

Table 1: *ALUOp* operation encoding

nected to each SLICEL input/output pin in Figure 1. You may fill each box in with one of the ALU BitSlice's inputs/outputs (a or c_{out}, for example), a constant logic 1/0, or label the input/output "*nc*" (not connected). You may or may not need all of the SLICEL logic provided.

Use as little logic as you can!

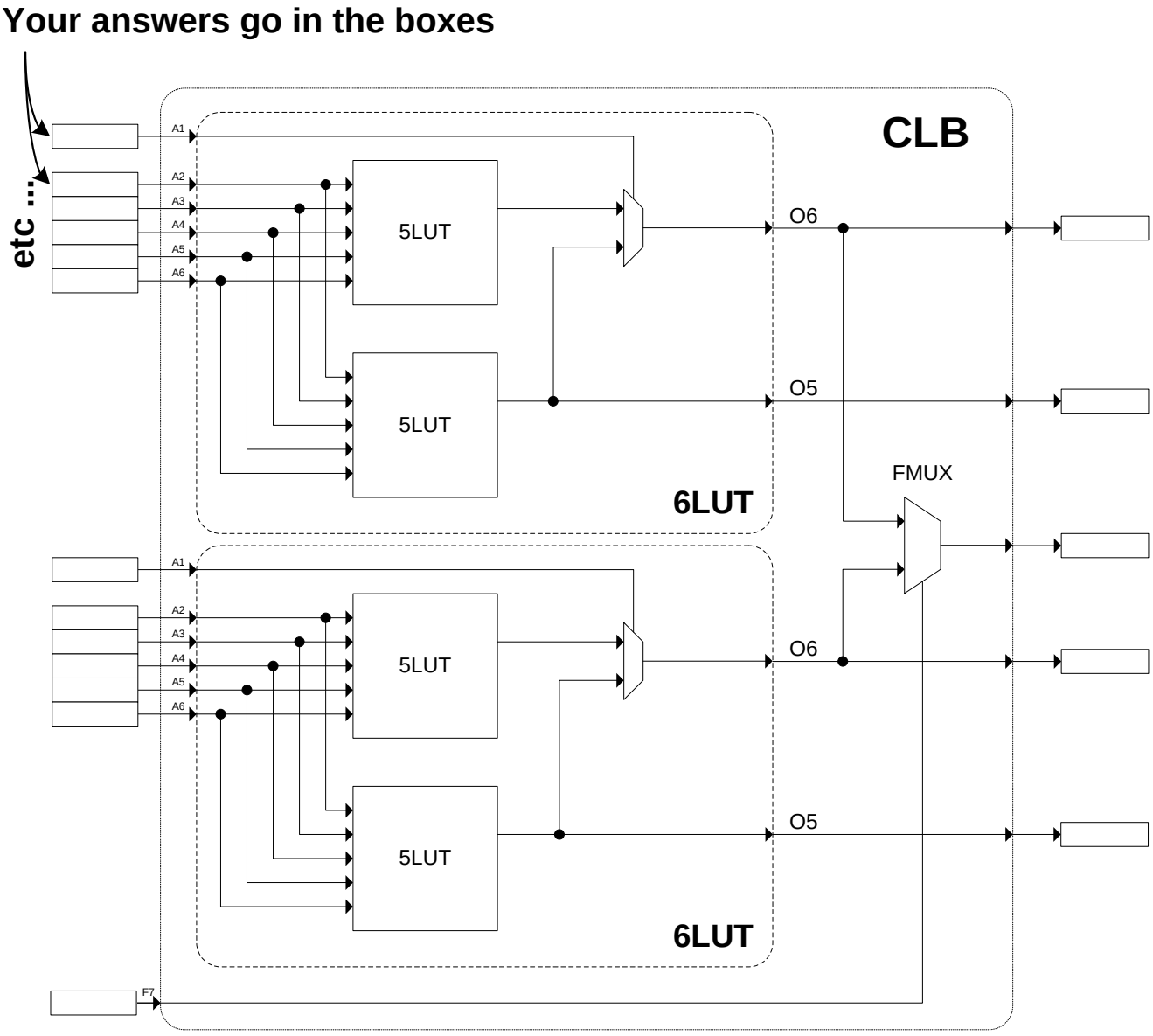

Figure 1: Simplified CLB.