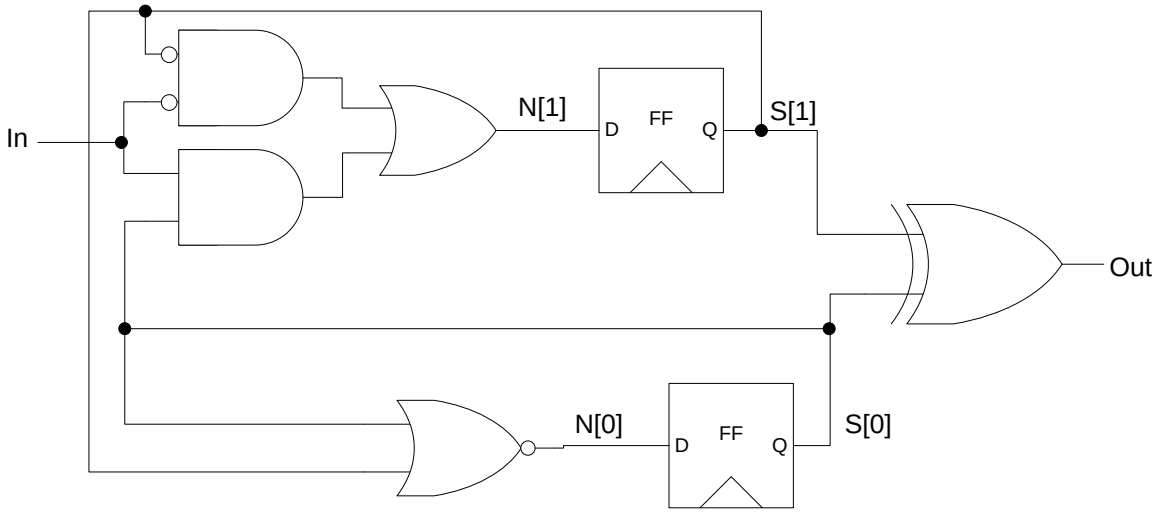
University of California at Berkeley
College of Engineering
Department of Electrical Engineering and Computer Science

EECS150, Spring 2010

Quiz 3: February 12^{th}

Consider the following circuit for questions 1-2:



1. Write a Verilog description of the circuit, using continuous assignment wherever possible.

```
module QuizCircuit(Clock, Reset, In, Out);
```

```
endmodule
```

2. Write a Verilog description of the circuit, using only always blocks.

```
module QuizCircuit(Clock, Reset, In, Out);
```

```
endmodule
```