University of California at Berkeley
College of Engineering
Department of Electrical Engineering and Computer Science

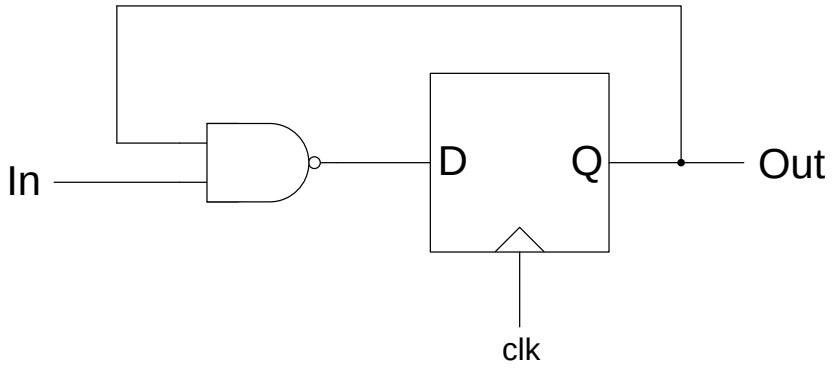
EECS150, Spring 2010

Quiz 4: February 19^{th}
Solution

The Verilog in this problem describes an FSM-like circuit with the following truth table:

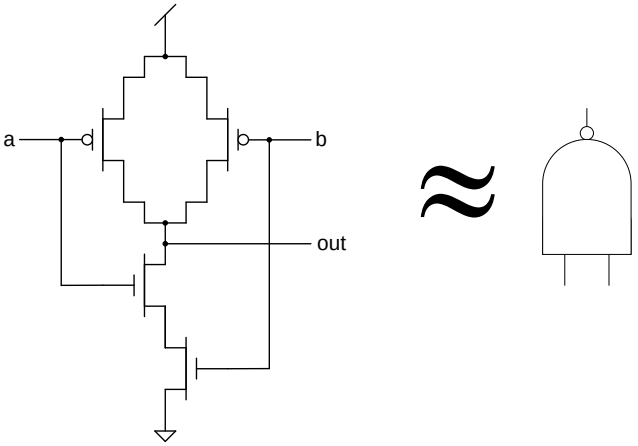
in	cs	ns
0	0	1
0	1	1
1	0	1
1	1	0

Upon examining the truth table, you should see that `ns` can be described using a simple *nand* gate! Thus, in terms of transistors, we need to build the *nand* and a flip-flop (which is, itself, built out of latches, which are, themselves, built out of transmission gates and inverters). The final FSM is shown here:

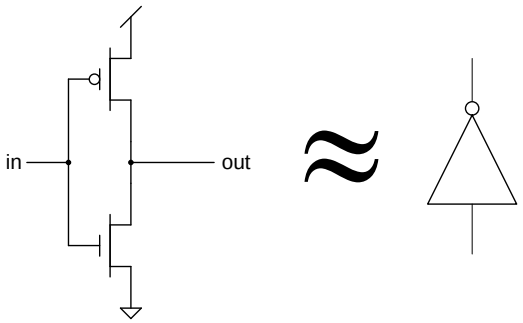


And the components used to build it are shown (in hierarchal order) on the next page.

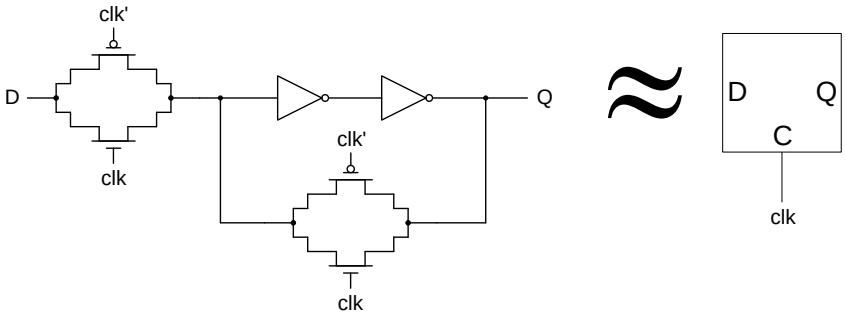
NAND Gate



Inverter



Latch



D-Q Flip-flop