University of California at Berkeley
College of Engineering
Department of Electrical Engineering and Computer Science

EECS150, Spring 2010

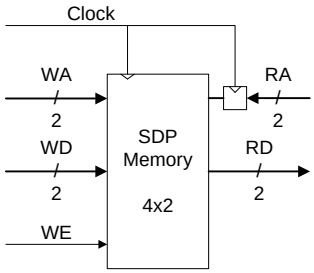
Quiz 6 SOLUTION: March 5^{th}
15 Minutes

Use **only** MUXes, gates, registers, and the memory primitive in the figure to answer the questions.

1. Consider a 4x2 simple dual port (SDP) SRAM memory with asynchronous reads. Add circuitry to make reads from this memory **synchronous**.
   Hint: draw a waveform for a synchronous read.

   Registering the output does not quite cut it: even though the read will indeed require a clock edge, the setup time suffers considerably. This approach is in disagreement with the definition of a synchronous read memory given in lecture.

   The correct solution registers the address input.



2. Implement a 8x2 **three-port** memory with 2 asynchronous read ports, and 1 write port. Use the space below.