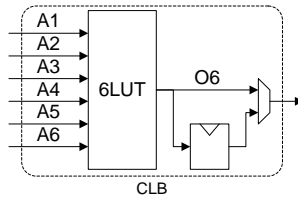


University of California at Berkeley
College of Engineering
Department of Electrical Engineering and Computer Science

EECS150, Spring 2010

Quiz 9: April 2nd
10 Minutes

Consider a system with generic FPGA architecture with 6-input LUTs and flip-flops, as shown below.



The timing characteristics of this system are detailed below:

- The shortest delay through the global routing fabric is 0.11 ns.
- The shortest delay through the 6LUT is 0.15 ns.
- The longest delay through the 6LUT is 0.53 ns.
- The delay through the MUX is 0.10 ns.
- The register Clock to Q delay is 0.47 ns.
- The flip-flop setup time is 0.15 ns.
- The flip-flop hold time is 0.24 ns.

Use this data to answer the following questions:

1. When building a 10 MHz processor, what is the largest number of consecutive LUTs allowed in one pipeline stage?
2. When building a shift register (using flip-flops), how much clock skew can the system tolerate without violating hold time?

Box and clearly label your answers. You may use the back of this quiz for overflow room.