Today: Graphics Processors

- **Computer Graphics.** A brief introduction to “the pipeline”.
- **Stream Processing.** Casting the graphics pipeline into hardware.
- **Unified Pipelines.** GeForce 8800, from Nvidia, introduced in 2006.
- **Kepler.** The latest generation from Nvidia, released a year ago.
PC Graphics, 2013 Edition
PC Graphics Architecture

Core i5 CPU/IGP

PCIe bus supports discrete GPU, with dedicated RAM and monitor outputs.

IGP uses system DRAM as graphics memory.

Display Out
About 12 MB/frame (24-bit pixels)
24 frames/sec: 300 MB/second
The “unaccelerated” graphics board...

Problem: CPU has to compute a new pixel every 10 ns. 10 clock cycles for a 1 GHz CPU clock.

300 MB/s easy to sustain.

Double Buffering:
- CPU writes A frame in one buffer.
- Control logic sends B frame out of other buffer to display.

Display Out

EECS 150: Graphics Processors

Tuesday, April 30, 13
Q. What kind of graphics are we accelerating?
A. In 2013, interactive entertainment (3-D games). In the 1990s, 2-D acceleration (fast windowing systems, games like Pac-Man).

Graphics Acceleration

Q. In a multi-core world, why should we use a special processor for graphics?
A. Programmers generally use a certain coding style for graphics. We can design a processor to fit the style.

Next: An intro to 3-D graphics.
The Triangle ...

Simplest closed shape that may be defined by straight edges.

With enough triangles, you can make anything.
A cube whose faces are made up of triangles. This is a 3-D model of a cube -- model includes faces we can’t see in this view.

A sphere whose faces are made up of triangles. With enough triangles, the curvature of the sphere can be made arbitrarily smooth.
A teapot (famous object in computer graphics history). A “wire-frame” of triangles can capture the 3-D shape of complex, man-made objects.
Triangle defined by 3 vertices

By transforming \( v' = f(v) \) all vertices in a 3-D object (like the teapot), you can move it in the 3-D world, change its size, rotate it, etc.

vertex \( v_0 = (x_0, y_0, z_0) \)

vertex \( v_1 = (x_1, y_1, z_1) \)

vertex \( v_2 = (x_2, y_2, z_2) \)

If a teapot has 10,000 triangles, need to transform 30,000 vertices to move it in a 3-D scene ... per frame!
Vertex can have color, lighting info ...

If vertices colors are different, this means that a smooth gradient of color washes across triangle.

vertex $v_0 = (r_0, g_0, b_0)$

vertex $v_1 = (r_1, g_1, b_1)$

vertex $v_2 = (r_2, g_2, b_2)$

More realistic graphics models include light sources in the scene. Per-vertex information can carry information about how light hits the vertex.
We see a 2-D window into the 3-D world

Let's follow one 3-D triangle.
From 3-d triangles to screen pixels

First, **project** each 3-D triangle that might “face” the “eye” onto the **image plane**.

Then, create “**pixel fragments**” on the **boundary** of the image plane triangle.

Then, create “**pixel fragments**” to **fill in** the triangle (**rasterization**).

**Why “pixel fragments”?** A screen pixel color might depend on many triangles (**example**: a glass teapot).
Process pixel fragment to “shade” it.

Algorithmic approach: Per-pixel computational model of metal and how light reflects off of it. Move teapot and what reflects off it changes.
Process each fragment to “shade” it.

Artistic approach: Artist paints surface of teapot in Photoshop. We “map” this “texture” onto each pixel fragment during shading.

Final step: Output Merge. Assemble pixel fragments to make final 2-d image pixels.
Real-world texture maps: Bike decals
Applying texture maps: Quality matters

“Good” algorithm. B and C look blurry.

“Better” algorithm. B and C are detailed.
Putting it All Together ...

Luxo, Jr: Short movie made by Pixar, shown at SIGGRAPH in 1986. First Academy Award given to a computer graphics movie.
Graphics Acceleration

Next: Back to architecture ...
The graphics pipeline in hardware (2004)

3-D vertex “stream” sent by CPU

Process each vertex

Create pixels fragments

Process pixel fragments

Output Merge

Programmable CPU “Vertex Shader”

Programmable CPU “Pixel Shader”

DirectX, OpenGL

PowerPC G4 microprocessor (L2 cache: 512K 1:1)

167 MHz MaxBus

AGP 4X bus

Algorithms are usually hardwired

To display
Vertex Shader: A "stream processor"

Vertex "stream" from CPU

- Only one vertex at a time placed in input registers.

From CPU: changes slowly (per frame, per object)

- Constant Registers (Read Only)
- Working Registers (Read/Write)

Input Registers (Read Only)

Shader CPU

- Shader Program Memory
  - Short (ex: 128 instr) program code.
  - Same code runs on every vertex.

Output Registers (Write Only)

Shader creates one vertex out for each vertex in.

Vertex "stream" ready for 3-D to 2-D conversion
Optimized instructions and data formats

128-bit registers, holding four 32-bit floats.

Typical use: \((x, y, z, w)\) representation of a point in 3-D space.

128-bit registers, holding four 32-bit floats.

Typical use: \((x, y, z, w)\) representation of a point in 3-D space.

The 1/sqrt() function is often used in graphics.

Typical instruction:

\[
\text{rsq dest src}
\]

\[
dest\{x, y, z, w\} = 1.0/\sqrt{\text{abs(src.w)}}.
\]

If \(src.w=0\), \(dest \rightarrow \infty\).
Easy to parallelize: Vertices independent

From CPU

Caveat: Care might be needed when merging streams.

Shader CPUs easy to multithread. Also, SIMD-like control.

Why?
3-D to 2-D may expect triangle vertices in order.

Input Registers

| x | y | z | w |

Shader CPU

Output Registers

| x | y | z | w |

To 3-D/2-D
Pixel shader specializations ...

Texture maps (look-up tables) play a key role.

Pixel shader needs fast access to the map of Europe on teapot (via graphics card RAM).

“Pixel Shader”

CPU
Pixel Shader: Stream processor + Memory

Pixel fragment stream from rasterizer

Indices into texture maps.

Engine does interpolation.

Texture Registers

Texture Engine

Register R0 is pixel fragment, ready for output merge

Register created one fragment out for each fragment in.

Shader creates one fragment out for each fragment in.

Shader CPU

From CPU: changes slowly (per frame, per object)

Input Registers (Read Only)

Only one fragment at a time placed in input registers.

Texture Registers

Memory System

Registers (Read/Write)
Example (2006): Nvidia GeForce 7900

278 Million Transistors, 650 MHz clock, 90 nm process

- Texture Cache
- 3-D to 2-D
- Vertex Shaders: 8
- Pixel Shaders: 24
- Output Merge Units

DVI/VGA/composite/S-video output port

EECS 150: Graphics Processors

UC Regents Spring 2013 © UCB

Tuesday, April 30, 13
Break Time ...
Basic idea: Replace specialized logic (vertex shader, pixel shader, hardwired algorithms) with many copies of one unified CPU design.

**Unified Architectures**

**Consequence:** You no longer “see” the graphics pipeline when you look at the architecture block diagram.

**Designed for:** DirectX 10 (Microsoft Vista), and new non-graphics markets for GPUs.
DirectX 10 (Vista): Towards Shader Unity

Earlier APIs: Pixel and Vertex CPUs very different ...

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Table 1: Shader model feature comparison summary.
Geometry Shader: Lets a shader program create new triangles.

Also: Shader CPUs are more like RISC machines in many ways.

Stream Output: Lets vertex stream recirculate through shaders many times ...
(and also, back to CPU)
Why? Particle systems ...
Why? Fractal images ...
Why? Position-Based Fluids
NVidia 8800: Unified GPU, announced Fall 2006

Thread processor sets shader type of each CPU

128 Shader CPUs

1.35 GHz Shader CPU Clock, 575 MHz core clock
Graphics-centric functionality ...

Texture engine and memory system

3-D to 2-D (vertex to pixel)

Pixel fragment output merge

Tuesday, April 30, 13
Can be reconfigured with graphics logic hidden...


1000s of active threads

3 TeraFlops Peak Performance
Ships with a C compiler.

Texture system set up to look like a conventional memory system (768MB GDDR3, 86 GB/s)
Optic Flow (Computer Vision)

Notate a movie with arrows to show speed and direction.
Chip Facts

90nm process
681M Transistors
80 die/wafer (pre-testing)

Design Facts

4 year design cycle
$400 Million design budget
600 person-years: 10 people at start, 300 at peak

A big die. Many chips will not work (low yield). Low profits.
GeForce 8800 GTX Card: $599 List Price

PCI-Express 16X Card - 2 Aux Power Plugs!

185 Watts Thermal Design Point (TDP) -- TDP is a "real-world" maximum power spec.
Some products are “loss-leaders”

Breakthrough product creates “free” publicity you can’t buy.

(1) Hope: when chip “shrinks” to 65nm fab process, die will be smaller, yields will improve, profits will rise.

(2) Simpler versions of the design will be made to create an entire product family, some very profitable.

“We tape out a chip a month”, NVidia CEO quote.
And it happened! 2008 nVidia products

<table>
<thead>
<tr>
<th></th>
<th>GTX 280</th>
<th>GTX 260</th>
<th>9800 GX2</th>
<th>9800 GTX+</th>
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**GTX 280**
- Price similar to 8800
- Stream CPU count > 2X

**9800 GPU**
- Specs similar to 8800
- Card sells for $199.
And again in 2012! GTX 680 -- “Kepler”

<table>
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<th>Spec</th>
<th>GTX 680</th>
<th>GTX 580</th>
<th>GTX 560 Ti</th>
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GTX 680
- 3X more effective CPUs as GTX 280, lower price point.
- 6X more CPUs as 8800, (from 2006).

GTX 560 Ti
- Specs better than GTX 280, sells for $249.
GTX 680

28nm process

3.5 billion transistors

1 GHz core clock

6GHz GDDR5

3 years, 1000 engineers
GTX 680

4X as many shader CPUs, running at 2/3 the clock (vs GTX 560).

Polymorph engine does polygon tessellation. PCIe bus no longer limits triangle count.

Tuesday, April 30, 13
History and Graphics Processors

Create standard model from common practice: Wire-frame geometry, triangle rasterization, pixel shading.

Put model in hardware: Block diagram of chip matches computer graphics math.

Evolve to be programmable: At some point, it becomes hard to see the math in the block diagram.

“Wheel of reincarnation” -- Hardwired graphics hardware evolves to look like general-purpose CPU. Ivan Sutherland co-wrote a paper on this topic in 1968!
Samaritan: Direct X-11 demo from Unreal. Runs in real-time on one GTX 680 (barely).
GPUs on mobile devices
iPad: iPhone++

A6X: ARMv7 cores, PowerVR GPUs

1 GB DRAM (128-bit interface)
Apple A6X

2012 iPad
CPU/IGP.

32 nm process,
10.4 x 11.9 mm

IGP fills
about 40% of die.

IGP: 2.5%
of Kepler
(in GFLOPs).
Mobile GPUs: Same ideas, scaled down.
Today: Graphics Processors

- **Computer Graphics.** A brief introduction to “the pipeline”.

- **Stream Processing.** Casting the graphics pipeline into hardware.

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- **Kepler.** The latest generation from Nvidia, released last month.