Last Time: Test plan for your project

Which testing types are good for each epoch?

Top-down testing
- complete processor testing
- processor testing with self-checks
- multi-unit testing
- unit testing

Bottom-up testing

Epoch 1
- unit testing early
- multi-unit testing later

Epoch 2
- processor testing with self-checks
- multi-unit testing
diagnostics

Epoch 3
- processor testing with self-checks
- multi-unit testing
diagnostics

Epoch 4
- complete processor testing verification
- processor testing with self-checks
diagnostics

Time

processor assembly complete
correctly executes single instructions
correctly executes short programs
Outline - Timing

- A clocked logic circuit primer
- Team networking break!
- More clocked logic circuits
Architects draw blocks...

Circuit designers draw ???

Improved Transistor Model: nFET

Logic is where they meet.
Architects reach logic top-down ...

wire next_R, next_Y, next_G;

assign next_R = rst ? 1'b1 : (change ? Y : R);
assign next_Y = rst ? 1'b0 : (change ? G : Y);
assign next_G = rst ? 1'b0 : (change ? R : G);

Is this structural Verilog?
EEs reach logic bottom-up ...

Small number of high-performance logic circuits.

For some definition of performance.

Can you build a processor entirely out of NAND gates?

Basic Components: CMOS Logic Gates
NOR Gate
NAND Gate

Out = A \cdot B

V_{dd}

Out

1/28/04

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Logic Synthesis bridges the gap

assign next_R = rst ? 1’b1 : (change ? Y : R);
assign next_Y = rst ? 1’b0 : (change ? G : Y);
assign next_G = rst ? 1’b0 : (change ? R : G);

It’s easier to work at one level of abstraction if you have a basic understanding of the level below.
Administrivia - Team Networking Break!

- Mini-Lab 2 this Friday (9/10).
  Remember to do the pre-lab!

- Lab 1 due Monday 9/13.

- First homework due 9/15.

- Lab 2 goes out on 9/14.
  The first team lab (next break)
A Logic Circuit Primer
Inverters: A simple transistor model

\[
\begin{array}{c|c}
\text{In} & \text{Out} \\
0 & 1 \\
1 & 0 \\
\end{array}
\]

pFET. A switch. “On” if gate is grounded.

nFET. A switch. “On” if gate is at Vdd.

Inverter

Circuit

\begin{align*}
\text{“0”} & \quad \text{In} \\
\text{“1”} & \\
\text{“0”} \\
\text{“1”} & \quad \text{Out}
\end{align*}

Vdd

PMOS

NMOS

In = \overline{\text{Out}}
Transistors as water valves

If electrons are water molecules, and a capacitor a bucket ...

A “on” p-FET fills up the capacitor with charge.

A “on” n-FET empties the bucket.
What is the bucket? A gate’s “fan-out”.

“Fan-out”: The number of gate inputs driven by a gate’s output.

Driving other gates slows a gate down.

Driving wires slows a gate down.
A closer look at fan-out ...

Driving more gates adds delay.

Linear model works for reasonable fan-out

Slope = 0.0021ns / fF

0.5ns

Cout
Propagation delay graphs ...

- Cascaded gates: 1->0

INV1

INV2

INV3

propagation delay for INV2 & INV3 in series
Intuition: Critical paths ...

T2 might be the critical (worst-case delay) path.

\[ x = g(a, b, c, d, e, f) \]

If \( d \) going 0-to-1 switches \( x \) 0-to-1, delay is \( T1 \).
If \( a \) going 0-to-1 switches \( x \) 0-to-1, delay is \( T2 \).

Would you be surprised if \( T1 > T2 \)? Why?
Why “might”? Wires have delay too ...

- Wires possess distributed resistance and capacitance

- Time constant associated with distributed RC is proportional to the square of the length

- Signals are typically “rebuffered” to reduce delay:
Team Networking Break!

Lab 2 goes out on 9/14. Time to form your team.

Optimal team size? Min/max?

Talk out little problems before they get big. Communicate.

Disagreements are inevitable. Build a bridge and get over it.
Clocked Logic Circuits
From Delay Models to Timing Analysis

Timing Analysis

What is the smallest T that produces correct operation?

<table>
<thead>
<tr>
<th>f</th>
<th>T</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 MHz</td>
<td>1 μs</td>
</tr>
<tr>
<td>10 MHz</td>
<td>100 ns</td>
</tr>
<tr>
<td>100 MHz</td>
<td>10 ns</td>
</tr>
<tr>
<td>1 GHz</td>
<td>1 ns</td>
</tr>
</tbody>
</table>
Timing Analysis and Logic Delay

Register:
An Array of Flip-Flops

Can T be smaller than worst-case delay through CL?
Flip Flops have internal delays ...

Value of $D$ is sampled on positive clock edge. Q outputs sampled value for rest of cycle.

t_setup

t_clk-to-Q
Conclusion -- Timing

- Logic delay: fan-out and wires
- Flip-flops: setup and clk-to-Q
- Critical path limits clock speed