CS152 – Computer Architecture and Engineering

Lecture 5 – Timing, Xilinx

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Last Time: Timing Analysis, Logic Delay

What is the smallest T that produces correct operation?

Worst case CL delay limits T.
Today’s Lecture - More Project Topics

- Clocked logic timing wrap-up
- Design Notebook
- Field Programmable Gate Arrays
Clocked Logic Timing
Flip Flops have internal delays ...

Value of D is sampled on positive clock edge.

Q outputs sampled value for rest of cycle.
Flip-Flop delays eat into “time budget”

How can we minimize FF overhead?

Note: we may not want to!

Combining Cell (symbol) is fully specified by:

Features

- Inputs
- Outputs
- Functions

Clk

- Internal
- External

Delay

- Fixed
- Programmable

Hold Time: Input must REMAIN stable after trigger clock edge

Clock-to-Q

- Clock-to-R
- Clock-to-Q

The time budget of a combinational logic stage is determined by the maximum delay through the stage.

cycle time is a function of the critical path

devices

Don’t Care

Data

don’t

Can

Input

transition

that

is

must be greater than:

Cycle time is a function of the critical path

Delay

- Fixed
- Programmable

Hold Time: Input must REMAIN stable after trigger clock edge

Clock-to-Q

- Clock-to-R
- Clock-to-Q

The time budget of a combinational logic stage is determined by the maximum delay through the stage.

T ≥ τ_{clk→Q} + τ_{CL} + τ_{setup}

ALU “time budget”

ALU “time budget”

T ≥ τ_{clk→Q} + τ_{CL} + τ_{setup}

T ≥ τ_{clk→Q} + τ_{CL} + τ_{setup}
Clock skew also eats into “time budget”

As $T \to 0$, which circuit fails first?

$$T \geq T_{\text{CL}} + T_{\text{setup}} + T_{\text{clk}\to Q} + \text{worst case skew}.$$
Some Flip Flops have “hold” time ...

\[ t_{\text{setup}} \quad t_{\text{hold}} \]

- Signal During \[ t_{\text{setup}}\] and \[ t_{\text{hold}}\] must stay stable.

\[ t_{\text{clk-to-Q}} + t_{\text{inv}} > t_{\text{hold}} \]

- Does flip-flop hold time affect operation of this circuit? Under what conditions?

\[ D \rightarrow Q \]

- CLK

- D must stay stable here.
Flip Flop delays: clk-to-Q? setup? hold?

CLK == 0
Sense D, but Q outputs old value.

CLK 0->1
Capture D, pass value to Q
Administrivia - Busy Week!

First homework due tomorrow!
283 Cory, in CS 152 box at 5 PM.

Lab 2 out today! Email project plan to TAs by Thursday @ 9 PM.

Appendix B reading added for Thursday’s lecture.

Final mini-Lab on Friday 9/17.
Don’t forget to do the pre-lab!

Also on Friday: TA project plan review. Revisions due 11:59 PM.
Xilinx FPGA Overview

Device Type
PQ208xxx0350
xxxxxxxxx
4C

Date Code
Lot Code

Temperature Range
Speed Grade
Package
Device Type

Spartan-3 FPGA Family: Introduction and Ordering Information
4 www.xilinx.com DS099-1 (v1.3) July 13, 2004
Prior Art for FPGAs ...
Xilinx: Large Array of CLBs, plus RAM

CLB == Configurable Logic Block
“Swiss Army Knife” part

From: Xilinx
Spartan 3 data sheet, modified to approximate Virtex architecture.
Blades in the CLB “Swiss Army Knife”

Look Up Table (LUT)

example $g(F1, F2, F3, F4): F1 \land F2 \land F3 \land F4$

Edge triggered flip-flop

Adder carry chain, multiplier step, LUT expansion logic.
Inside a LUT ...

<table>
<thead>
<tr>
<th>INPUTS</th>
<th>INPUTS</th>
</tr>
</thead>
<tbody>
<tr>
<td>0000</td>
<td>(g(0,0,0,0))</td>
</tr>
<tr>
<td>0001</td>
<td>(g(0,0,0,1))</td>
</tr>
<tr>
<td>0010</td>
<td>(g(0,0,1,0))</td>
</tr>
<tr>
<td>0011</td>
<td>(g(0,0,1,1))</td>
</tr>
<tr>
<td>0100</td>
<td>(\cdot)</td>
</tr>
<tr>
<td>0101</td>
<td>(\cdot)</td>
</tr>
<tr>
<td>0110</td>
<td>(\cdot)</td>
</tr>
<tr>
<td>0111</td>
<td></td>
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<tr>
<td>1000</td>
<td></td>
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<td>1100</td>
<td></td>
</tr>
<tr>
<td>1101</td>
<td></td>
</tr>
<tr>
<td>1110</td>
<td></td>
</tr>
<tr>
<td>1111</td>
<td></td>
</tr>
</tbody>
</table>

Part of a FF “scan chain”

Set during configuration.

To next FF in chain ...
After routing ...
Xilinx: Large Array of CLBs, plus RAM

Clus

plus wires

IOBs

CLBs

IOBs

CLBs

Block RAM

CLB

From: Xilinx
Spartan 3 data sheet, simplified.
Wiring CLBs together...

Set during configuration.

Why use different wiring patterns?

A “cross-point connection”

Occupies wiring channels...

(not all wires shown)
Clocks have dedicated wires (low skew)

From: Xilinx Spartan 3 data sheet. Virtex is similar.
Die photo:
Xilinx Virtex

Calinx:
38,400 LUT + FF + adder

655 kb block RAM
The analogy holds up ...

CLBs are “real” elements, with real physics. Not a simulation of physics.

Configurability has a price: lower performance, wasted resources.
Let synthesis do the heavy lifting ...

```vhdl
assign next_R = rst ? 1'b1 : (change ? Y : R);
assign next_Y = rst ? 1'b0 : (change ? G : Y);
assign next_G = rst ? 1'b0 : (change ? R : G);
```

Avoid the temptation to get too close to the LUTS and wiring channels
**Conclusions**

- **Timing key concept:** critical path
- **Keep a good Design Notebook!**
- **Xilinx:** Physical, yet configurable