You Are Here

Lab 3
Final Report
Due

FINAL
PROJECT
FINAL
DESIGN DOC

FINAL
PROJECT
PRELIM
DESIGN DOC

FINAL
PROJECT
DRAM
CHECKOFF
Midterm II
6-9 PM
306 SODA

Final Project Talks

The End
Two parts to the rest of semester

**Pre-Thanksgiving:** Lab 3 and the Final Project are your only responsibilities.

**Post-Thanksgiving:** HW 2 due, Midterm II, “Lessons Learned” time-capsule talks for future CS152s.

So, what is the purpose of lectures going forward?
Next 2 weeks: Prepare you for final project (cache + DRAM)

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Rest of Semester: Advanced Topics ...
Recent history of CS 152 ...

Failed projects: In Fall 04 and Spring 05, many groups didn’t get their final project CPU working (80% didn’t work in Fall 04, 50% didn’t work in Spring 05). In Fall 05, all groups got their final project working in hardware (some did not pass all tests).

Our goal for Fall 06:

All projects successful: We want every group to get every CPU working.
Today: State Storage Tools on Silicon ICs

Capacitance: Holds state as charge

Transistors: How to move charge

Layout: How to fabricate your IC

DRAM: 1 Transistor + 1 Capacitor

VLSI == “Very Large Scale Integration”

The tall thin designer, with feet on the ground and head in the sky.

The ground: Physics and IC Fabrication
The sky: Architecture and Applications

Carver Mead
Capacitance
Recall: Building a capacitor

Top Plate

Conducts electricity well. (metal, doped polysilicon)

Dielectric

An insulator. Does not conduct electricity at all. (air, glass (silicon dioxide))

Bottom Plate

Conducts electricity well (metal, doped polysilicon)
Recall: Capacitors in action

Because the dielectric is an insulator, and does not conduct.

$I = 0$

After circuit “settles” ...

$Q = CV = C \times 1.5$ Volts (D cell)

$Q$: Charge stored on capacitor

$C$: The capacitance of the device: function of device shape and type of dielectric.

After battery is removed:

Still, $Q = C \times 1.5$ Volts

Capacitor “remembers” charge
Capacitors and current ...

\[ Q = C \ V \]

Differentiate with respect to time ... if \( C \neq C(t) \) ...

\[ \frac{dQ}{dt} = C \ \frac{dV}{dt} \]

I is defined as \( \frac{dQ}{dt} \) ...

\[ I = C \ \frac{dV}{dt} \]

Observation: If a voltage change \( dV \) occurs in zero time \((dt = 0)\), the current \( I \) is infinite (impossible).

The voltage across a capacitor cannot change instantaneously. And by \( Q = C \ V \), the charge stored on a capacitor cannot change instantaneously.
State is coded as the amount of energy stored by a device.

State is read by sensing the amount of energy

Problems: noise changes $Q$ (up or down), parasitics leak or source $Q$. Fortunately, $Q$ cannot change instantaneously, but that only gets us in the ballpark.
How do we fight noise and win?

Store more energy than we expect from the noise.

Q = CV. To store more charge, use a bigger V or make a bigger C. Cost: Power, chip size.

Represent state as charge in ways that are robust to noise.

Example: 1 bit per capacitor. Write 1.5 volts on C. To read C, measure V. V > 0.75 volts is a “1”. V < 0.75 volts is a “0”.

Cost: Could have stored many bits on that capacitor.

Correct small state errors that are introduced by noise.

Cost: Complexity.

Ex: read C every 1 ms. Is V > 0.75 volts? Write back 1.5V (yes) or 0V (no).
MOS Transistors

Two diodes and a capacitor in an interesting arrangement. So, we begin with a diode review ...
Diodes in action ...

Resistor

Light emitting diode (LED)

Light on?

Yes!

No!
Diodes: Current vs Voltage

Anode

Cathode

Diode is off

$I \approx -I_0$

Diode is on

$I \approx I_0 \exp(V/V_0)$

$I = I_0 \left[ \exp(V/V_0) - 1 \right]$

$I_0$ range: 1fA to 1nA

$V_0$ range: 25mV to 60 mV
Making a diode on a silicon wafer
A pure ("intrinsic") silicon crystal ...

Conducts electricity better than an insulator, worse than a conductor.

Why? Most electrons (dots) are in a full "valence" band. Moving in the band is difficult.
Especially near 0 degrees K.

Lots of room, but few electrons.

Forbidden "band gap"

Many electrons, but packed too tight to move.
Intrinsic silicon crystal as $T$ rises ...

Some valence band electrons diffuse into the conduction band.

These electrons leave behind "holes" in the valence band, allowing remaining electrons to move easier.

We think of "holes" as positive carriers...

More electrons, better conduction
We “engineer” crystal with impurities ...
N-type silicon: add donor atoms

Use diffusion or ion implantation to replace some of the Si atoms with As

Arsenic has an extra electron that is "donates" to the conduction band.


Electrons from donor atoms. Improves conductivity.

Donor energy

Conduction band

Valence band

No change in the number of holes
P-type silicon: add acceptor atoms

Use diffusion or ion implantation to replace some of the Si atoms with Boron.

Boron has one fewer electron than Si. It can accept valence band electrons, creating holes.

\( p^+ \): heavy doping. \( p^- \): light doping.

No change in conduction band electron count.

Number of holes increased, conductivity improves.

Boron Atom

Valence band

Conduction band

Acceptor energy

p-type silicon: add acceptor atoms
How to make a silicon diode...

At $V \approx 0$, “hill” too high for electrons to diffuse up.

For holes, going “downhill” is hard.

$V$ controls hill.
Diodes: Current vs Voltage

Diode is off
\[ I = -I_0 \]

Diode is on
\[ I = I_0 \exp\left(\frac{V}{V_0}\right) \]

Io range: 1fA to 1nA
Vo range: 25mV to 60 mV
Note: IC Diodes are biased “off”!

V1, V2 > 0V. Diodes “off”, only current is Io “leakage”.

\[ I = Io \left[ \exp \left( \frac{V}{V_o} \right) - 1 \right] \]

Anodes of all diodes on wafer connected to ground.
Based on Fall 05 Mid-term II ...

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- Lab 3: Final Design Document due to TAs, 11:59PM
- HW 2 available (due at Midterm II review session)
- Lab 3: Initial Xilinx Checkoff, 12-2PM or 3-5PM, 125 Cory

Xilinx checkoff: Pipelining w/o the hard parts ...
MOS Transistors

Two diodes and a capacitor in an interesting arrangement ...
What we want: the perfect switch.

We want to turn a p-type region into an n-type region under voltage control.

We need electrons to fill valence holes and add conduction band electrons.

Switch is off. V1 is not connected to V2.

Switch is on. V1 is connected to V2.

What we want: the perfect switch.
An n-channel MOS transistor (nFET)

\[
\begin{align*}
V_d &= 1\text{V} \\
V_g &= 0\text{V} \\
V_s &= 0\text{V}
\end{align*}
\]

- Polysilicon gate, dielectric, and substrate form a capacitor.
- nFet is off (I is “leakage”)

\[
\begin{align*}
V_d &= 1\text{V} \\
V_g &= 1\text{V} \\
V_s &= 0\text{V}
\end{align*}
\]

- Vg = 1V, small region near the surface turns from p-type to n-type.
- nFet is on.
Drawing an nFET

“Mask” drawings sent to the fabrication facility to make the chips.
Mask set for an n-Fet (circa 1986)

Vd = 1V
Vg = 0V
Vs = 0V

Top-down view:

Masks:
#1: n+ diffusion
#2: poly (gate)
#3: diff contact
#4: metal

Layers to do p-Fet not shown. Modern processes have 6 to 10 metal layers (or more) (in 1986: 2).
"Design rules" for masks, 1986...

Poly overhang. So that if masks are misaligned, we still get "---" in channel.

Minimum gate length. So that the source and drain depletion regions do not meet!

Metal rules: Contact separation from channel, one fixed contact size, overlap rules with metal, etc...

#1: n+ diffusion
#2: poly (gate)
#3: diff contact
#4: metal
Fabrication
Mask set for an n-Fet ...

Vd = 1V  \quad Vg = 1V  \quad Vs = 0V

Top-down view:

Masks

#1: n+ diffusion
#2: poly (gate)
#3: diff contact
#4: metal

How does a fab use a mask set to make an IC?
Start with an un-doped wafer ... 

UV hardens exposed resist. A wafer wash leaves only hard resist.

Steps

#1: dope wafer p-

#2: grow gate oxide

#3: grow undoped polysilicon

#4: spin on photoresist

#5: place positive poly mask and expose with UV.
Wet etch to remove unmasked ...

HF acid etches through poly and oxide, but not hardened resist.

After etch and resist removal
Use diffusion mask to implant n-type accelerated donor atoms

Notice how donor atoms are blocked by gate and do not enter channel.

Thus, the channel is "self-aligned", precise mask alignment is not needed!
Metallization completes device

Grow a thick oxide on top of the wafer.

Mask and etch to make contact holes.

Put a layer of metal on chip. Be sure to fill in the holes!
Final product ...

Top-down view:

Vd |
----|
| p- |
| η+ |
|    |
oxide
| η+ |
|    |
| Vs |

“The planar process”
Jean Hoerni,
Fairchild Semiconductor
1958
p-channel Transistors
p-Fet: Change polarity of everything

\[
V_{well} = V_s = 1V \quad V_g = 0V \quad V_d = 0V
\]

Isd = \mu A

"Mobility" of holes is slower than electrons.

p-Fets drive less current than n-Fets, all else being equal.
Device Equations
Recall: Our old “switch” model ...

We begin by modeling transistors that are “off”

A “on” p-FET fills up the capacitor with charge.

A “on” n-FET empties the bucket.
Recall: Why diode current is $I = \exp(V)$ ...

At $V = 0$, “hill” too high for electrons to diffuse up. For holes, going “downhill” is hard.

$V$ controls hill.
A simple model for "off" transistor ...

\[
\begin{align*}
V_d &= 1\text{V} \\
V_g &= 0.2\text{V} \\
V_s &= V_{\text{sub}} = 0\text{V}
\end{align*}
\]

\[
\text{Ids} = I_0 \left[ \exp\left(\frac{\kappa V_g - V_s}{V_o}\right) \right] \left[ 1 - \exp\left(-\frac{V_d}{V_o}\right) \right]
\]

\[
I_0 \approx 1\text{fA}, \quad V_o = kT/q = 25\text{mV}, \quad \kappa = 0.7
\]

Current flows when electrons diffuse to the "gate wall" top

\# electrons that reach top goes up as wall comes down, implies \( \text{Ids} \sim \exp(V_g) \)
From Lecture 6: Leakage current

Even when a logic gate isn't switching, it burns power.

\[ 0V = V_{IN} \]

\[ I_{Gate}, I_{Sub}, V_{OUT} \]

\( I_{sub} \): Even when this nFet is off, it passes an \( I_{off} \) leakage current.

We can engineer any \( I_{off} \) we like, but a lower \( I_{off} \) also results in a lower \( I_{on} \), and thus the lower the clock speed.
From Lecture 6: Transistor Off Current

\[ I_{ds} = I_0 \left[ \exp\left(\frac{kV_g - V_s}{V_0}\right) \right] \left[ 1 - \exp\left(-\frac{V_{ds}}{V_0}\right) \right] \]

\( I_{off} \approx 10 \text{ nA} \)

1.2 mA = \( I_{on} \)

0.25 = \( V_T \)

0.7 = \( V_{dd} \)
Simple model for “on” transistor ...

\[ V_{d} = 2V \quad V_{g} = 1V \quad V_{s} = V_{\text{sub}} = 0V \]

\[ I_{\text{d}} = \mu A \quad \text{dielectric} \]

\[ I_{\text{d}} = (\text{carriers in channel}) / (\text{transit time}) \]

\[ Q = CV \quad f(\text{length, velocity}) \]

\[ I_{\text{d}} = \left[ \frac{(\mu \epsilon W)}{(LD)} \right] \left[ V_{gs} - V_{th} \right] \left[ V_{ds} \right] \]

If \( V_{ds} > V_{gs} - V_{th} \), channel physics change:

\[ I_{\text{d}} = \left[ \frac{(\mu \epsilon W)}{(2LD)} \right] \left[ V_{gs} - V_{th} \right]^2 \]

\[ W = \text{transistor width, } L = \text{length,} \]

\[ D = \text{capacitor plate distance} \]

\[ \mu \text{ is velocity, } \epsilon \text{ is C dielectric constant} \]
From Lecture 6: Transistor On Current

\[ I_{ds} = \left( \frac{\mu V}{2LW} \right) [V_{gs} - V_{th}]^{1.x} \]

25nm is a small device! The simple model no longer captures how “on” device works.

\[ I_{off} = 0 \] ???

\[ V_t = 0.25 \]

\[ V_{dd} = 0.7 \]

\[ 1.2 \text{ mA} = I_{on} \]
Dynamic Memory (DRAM)
Recall: Capacitors in action

Because the dielectric is an insulator, and does not conduct.

After circuit “settles” ...

- $Q = C \times V = C \times 1.5$ Volts (D cell)
- $Q$: Charge stored on capacitor
- $C$: The capacitance of the device: function of device shape and type of dielectric.

After battery is removed:

Still, $Q = C \times 1.5$ Volts

Capacitor “remembers” charge
DRAM cell: 1 transistor, 1 capacitor

Word Line and Vdd run on “z-axis”

Why Vcap values start out at ground. Diode leakage current.
A 4 x 4 DRAM array (16 bits) ....
Invented after SRAM, by Robert Dennard

United States Patent Office

3,387,286
Patented June 4, 1968

FIELD-EFFECT TRANSISTOR MEMORY
Robert H. Dennard, Croton-on-Hudson, N.Y., assignor to International Business Machines Corporation, Armonk, N.Y., a corporation of New York
Filed July 14, 1967, Ser. No. 653,415
21 Claims. (Cl. 340—173)

FIG. 1

FIG. 2

Inventent in disclosing various concepts and structures which have been developed in the application of field-effect transistors to different types of memory applications, the primary thrust up to this time in conventional read-write random access memories has been to connect a plurality of field-effect transistors in each cell in a latch configuration. Memories of this type require a large number of active devices in each cell and therefore each cell re-
**DRAM Circuit Challenge #1: Writing**

Vdd - Vth. Bad, we store less charge. Why do we not get Vdd?

\[ I_{ds} = \frac{\mu \varepsilon W}{2Ld} (V_{gs} - V_{th})^2 \]

but "turns off" when \( V_{gs} \leq V_{th} \)!

Vgs = Vdd - Vc. When Vdd - Vc \( \leq \) Vth, charging effectively stops!
DRAM Challenge #2: Destructive Reads

Raising the word line removes the charge from every cell it connects too!

Must write back after each read.
Assume $C_{cell} = 1 \, \text{fF}$

Word line may have 2000 nFet drains, assume word line $C$ of 100 fF, or $100 \times C_{cell}$.

$C_{cell}$ holds $Q = C_{cell} \times (V_{dd} - V_{th})$

When we dump this charge onto the word line, what voltage do we see?

$dV = \frac{C_{cell} \times (V_{dd} - V_{th})}{100 \times C_{cell}}$

$dV = \frac{(V_{dd} - V_{th})}{100} = \text{tens of millivolts!}$

In practice, scale array to get a 60mV signal.
DRAM Circuit Challenge #3b: Sensing

How do we reliably sense a 60mV signal?

Compare the word line against the voltage on a "dummy" world line.

"Dummy" word line. Cells hold no charge.

Word line to sense

Dummy word line

"sense amp"
DRAM Challenge #4: Leakage ...

Parasitic currents leak away charge.

Solution: "Refresh", by reading cells at regular intervals (tens of milliseconds)

Diode leakage...
Cell capacitor holds 25,000 electrons (or less). Cosmic rays that constantly bombard us can release the charge!

Solution: Store extra bits to detect and correct random bit flips (ECC).
Extra word lines. Used for “sparing”.

If one bit is bad, do we throw chip away?

Solution: add extra word lines (i.e. 80 when you only need 64). During testing, find the bad word lines, and use high current to burn away “fuses” put on chip to remove them.
From Lecture 6: Process Scaling

Recall process scaling ("Moore’s Law") from Lecture 2...

Due to reducing $V$ and $C$ (length and width of $C_s$ decrease, but plate distance gets smaller).

Recent slope more shallow because $V$ is being scaled less aggressively.

Each generation of IC technology, we shrink width and length of cell.

As $C_{cell}$ and drain capacitances scale together, number of bits per word line stays constant.

$$dV = 60 \text{ mV} = \frac{C_{cell}(V_{dd} - V_{th})}{100 \times C_{cell}}$$

Problem 1: Number of arrays per chip grows!

Problem 2: $V_{dd}$ may need to scale down too!

Solution: Constant Innovation of Cell Capacitors!
Poly-diffusion Ccell is ancient history

Word Line and Vdd run on “z-axis”
Modern cells: “trench” capacitors

Figure 4

SEM photomicrograph of 0.25-μm trench DRAM cell suitable for scaling to 0.15μm and below. Reprinted with permission from [17]; © 1995 IEEE.
Modern cells: “stacked” capacitors
Lessons (re)learned

- Capacitors hold state
- Semiconductor physics
- Drawing transistors
- Transistor wrap-up: Fabrication, p-FETs, device model equations.
- DRAM: 1 Transistor + 1 Capacitor
Lectures: Coming up next ...

Memory array structures and interfaces.

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The memory hierarchy