(1) Threads on two cores that use shared libraries conserve L2 memory.

(2) Threads on two cores share memory via L2 cache operations. Much faster than 2 CPUs on 2 chips.
今日：公共传输线，硬盘和RAID

**公共传输线：** 共享的物理线路，被用于在多个设备（通常称为“外围设备”）之间传输信号。

公共传输线让电脑可以被扩展：添加更多的内存，更好的显卡，网络摄像头等。

**硬盘：** 存储位作为微型“条形磁铁”在旋转磁盘的排列。机械设备：缓慢且容易出错。

---

CS 152 L23: Buses, Disks, and RAID
Properties of bus structures ...

Control lines: Controls transactions, signals what is on data lines

Data lines: Carries information across the interface

Buses are an abstraction for communication: helps designers compose large, complex systems.
### Buses are defined in layers ...

---

#### Example: DIMM DRAM bus. The name of every wire is defined in a standards document.

- **Transaction Protocols**
- **Signal Timing on Wires**
- **Wires**
- **Electrical Properties**
- **Mechanical Properties**

---

Lower levels of DRAM bus specification

Transaction Protocols

Signal Timing on Wires

Wires

Electrical Properties

Mechanical Properties

Table 9: Trace Length Table for Clock Topologies

<table>
<thead>
<tr>
<th>Segment</th>
<th>L0</th>
<th>L1</th>
<th>L2</th>
<th>L3</th>
<th>L4</th>
<th>Total Min</th>
<th>Total Max</th>
</tr>
</thead>
<tbody>
<tr>
<td>Length</td>
<td>0.10</td>
<td>1.00</td>
<td>0.80</td>
<td>0.50</td>
<td>0.10</td>
<td>2.45</td>
<td>2.55</td>
</tr>
<tr>
<td>Tolerance</td>
<td>± 0.05</td>
<td>± 0.02</td>
<td>± 0.02</td>
<td>± 0.02</td>
<td>± 0.05</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Layer</td>
<td>Outer</td>
<td>Inner</td>
<td>Inner</td>
<td>Inner</td>
<td>Outer</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Ideally, DIMMs made by any manufacturer should fit into any compliant socket, and work.
Upper levels of DRAM bus specification

<table>
<thead>
<tr>
<th>SYMBOL*</th>
<th>-7E MIN</th>
<th>-7E MAX</th>
<th>-75 MIN</th>
<th>-75 MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>TAC (3)</td>
<td>5.4</td>
<td>5.4</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>TAC (2)</td>
<td>5.4</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>TAH</td>
<td>0.8</td>
<td>0.8</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>TAS</td>
<td>1.5</td>
<td>1.5</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>TCH</td>
<td>2.5</td>
<td>2.5</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>TCL</td>
<td>2.5</td>
<td>2.5</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>TCK (3)</td>
<td>7</td>
<td>7</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>TCK (2)</td>
<td>7.5</td>
<td>10</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>TCKH</td>
<td>0.8</td>
<td>0.8</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
</tbody>
</table>

Collaboration between DRAM manufacturers (Samsung, Micron) and DRAM users (Intel, Cisco, ...).

Transaction Protocols

Signal Timing on Wires

Wires

Electrical Properties

Mechanical Properties

CS 152 L23: Buses, Disks, and RAID
Bus wires shared between many DIMMS

Apple Xserve G5 - has 8 DIMM slots, to support 8GB.

DIMMs respond to transaction requests. Since memory controller is only bus master, and there are a small number of DIMM slots, bus sharing is easy: use dedicated wires to each slot.

Memory controller is the only "bus master" - it can start transactions on the bus, but the DIMMs cannot.
Buses: pros and cons ...

+++ Low cost. One set of wires from memory controller can support up to 8 DIMMs.

--- Latency of bus increases with length of wires (needed to reach all 8 DIMM sockets), and the loading of 8 DIMMs. Must design for worst-case (8 DIMMs), even if only 1 DIMM is present.

--- Shared wires limit maximum bandwidth from memory. If memory controller had 8 sets of dedicated wires, one per DIMM, memory bandwidth would be much better (but more expensive).
Buses turn a CPU into a product

Case Study: Mac Mini
Constraints: Size, low price (499 USD)

Size fixed by the “form factor” (physical size) of desktop DIMMS. Laptop DRAM is smaller, but too expensive for $499 price.
Users expansion via serial buses

Serial: Data is sent “bit by bit” over one logical wire.

Serial pros and cons:

+++ Sending data over many wires introduces “skew” - signals travel on each wire at a slightly different speed. Skew limits speed and length of a bus. Serial buses have fewer skew issues, because they only use one logical wire.

+++ Low cost: a small number of wires cost less. Also, cheap wires and connectors can be used, since skew is less a problem.

--- When only using one wire, there is a bandwidth limit. Thus, DIMMs uses many wires (a ”parallel” bus, not “serial”).

USB, FireWire, Ethernet.
Many other buses hidden from user


Bus controller. Just 1 for low cost. High-end products have two: fast North Bridge, slow South Bridge.

**CPU: PowerPC G4 (Freescale)**

- **DVI/VGA/composite/S-video output port**
- **FireWire 400 port**
- **Ethernet port 10/100 Mbps**
- **Headphone/audio line-out jack**
- **USB 2.0 port (480 Mbps)**
- **USB 2.0 port (480 Mbps)**
- **Modem port**

CS 152 L23: Buses, Disks, and RAID

UC Regents Spring 2005 © UCB
Uses many standard parallel buses...

**AGP 4X bus.**
Graphics chip.

**ATA/100 bus.**
For hard disk, DVD/CD ROM.

**PCI, ATA, AGP devices can be bus master, for Direct Memory Access (DMA).**
Disk can write RAM directly.
ATI Radeon 9200 GPU

VRAM Chip 1

North/South chipset
Reminder: Friday DRAM controller checkoff

Run your test vector suite on the Calinx board, display results on LEDs.

Test ongoing transactions on both buses, with randomized start times. Load, store, and verify different data word patterns.
Disks
Trick: use bar magnets to code bits
Write and read bar direction on a disk

**Longitudinal Recording:**

Today’s technology. Magnets tend to erase each other.

**Perpendicular Recording:**

Coming soon.
Read head signal from spinning disk ...
Each ring is a "track".

A track is divided into "sectors".

A sector codes a fixed # of bytes (ex: 4K blocks).

Outer tracks hold more sectors.

2005 desktop rotation speed: 7200 RPM
A "seek": When the arm is moved so that the heads are over the desired track.

"Seek time": Average time to move from one track to another track. Pessimistic estimate of real-world performance. 2005 desktop drive typical seek time: 8.5 milliseconds.
Disk Latency Equation

Latency of a disk block read =

Queueing Time +

Controller Time +

Seek Time +

Rotation Time +

Transfer Time

Zero if no other accesses pending.

Usually short.

2005: about 8 ms

4.2 ms @ 7200 RPM

1/2 full rotation time

1 ms @ 7200 RPM
A Case for Redundant Arrays of Inexpensive Disks (RAID)

David A. Patterson, Garth Gibson, and Randy H. Katz

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Department of Electrical Engineering and Computer Sciences
571 Evans Hall
University of California
Berkeley, CA 94720
(patterson@ginger.berkeley.edu)
Why disk arrays? Reliability + throughput

with duplicated paths, higher performance can be obtained when there are no failures

Goal: No Single Points of Failure

host

I/O Controller

Fully dual redundant

I/O Controller

host

Array Controller

Array Controller

Disk(s) can fail in a group w/o losing access to the data stored in the group.

Recovery Groups (columns)
RAID Level: Recovery Group Organization

RAID 1: Disk Mirroring

5-disk Recovery Group

D0

D1

D2

D3

D4

B0 B1 B2 \ldots

B0 B1 B2 \ldots

B0 B1 B2 \ldots

B0 B1 B2 \ldots

Logical Blocks Bn on Array

Each disk holds a copy of each block.

+++ High availability.

+++ High read bandwidth.

--- High disk capacity cost.
Recall from ECC lecture: Parity Codes

Simple case: Two 1KB blocks of data (A and B)

Create a parity block, P: “Parity codes”

\[ P = A \oplus B \text{ (do } \oplus \text{ on each bit of block)} \]

Read all three blocks. If A or B is not available but P is, regenerate A or B:

\[ A = P \oplus B \]
\[ B = P \oplus A \]

The math is easy: the trick is system design!
Examples: RAID, voice-over-IP parity FEC.
For lower capacity cost: parity codes

RAID 3: Parity Disk

80% of disks hold unique data

+++ Low cost.

--- Only one disk may fail.

--- Pdisk limits write bandwidth

--- No read bandwidth gain.

5-disk Recovery Group

D0

D1

D2

D3

Parity

B0 B4 B8 ...

B1 B5 B9 ...

B2 B6 B10 ...

B3 B7 B11 ...

P0 P1 P2 ...

Logical Blocks Bn on Array
Improve write performance: Interleave P

RAID 5: Interleaved Parity Disks

+++ Writes of parity blocks distributed across 5 disks

COD/e3
Page 574-580 for RAID details.

Will be responsible for level of detail in book for Mid-term II.
Conclusions: Buses, Disks, and RAID

Buses make the machine. “Value” and “high-end” machines may have similar CPUs, different chip-sets.

Disks are different: As mechanical devices, they move on a millisecond time frame, and suffer mechanical failure. System design must cope with this reality, not ignore it.