The following comment is from the source code of MIPS/Linux and, despite its cryptic terminology, describes a three-level page table.

```
/*
 * Each address space has 2 4K pages as its page directory, giving 1024
 * 8 byte pointers to pmd tables. Each pmd table is a pair of 4K pages,
 * giving 1024 8 byte pointers to page tables. Each (3rd level) page
 * table is a single 4K page, giving 512 8 byte ptes.
 * /
```

Assuming 4K pages, how long is each index?

<table>
<thead>
<tr>
<th>Index</th>
<th>Length of index (bits)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Top-level (“page directory”)</td>
<td></td>
</tr>
<tr>
<td>2nd-level</td>
<td></td>
</tr>
<tr>
<td>3rd-level</td>
<td></td>
</tr>
</tbody>
</table>

**Problem S6.2**

Variable Page Sizes

A TLB may have a page mask field that allows an entry to map a page size of any power of four between 4KB and 16MB. The page mask specifies which bits of the virtual address represent the page offset (and should therefore not be included in translation). What are the maximum and minimum reach of a 64-entry TLB using such a mask?