Agenda

• Lab 2
• Cache Review
• Virtual Memory
Lab 2

- Is out now!
- Due March 1st

- Simulate memory hierarchy using Simics
  - simulations will take much longer
  - using real benchmarks running on a real OS
Simics

- a “full-system” ISA simulator
  - runs the **entire software stack** (OS, bootloader, apps)
  - very, VERY **fast** speeds
    - (relative to real hardware, anyways)
- designed for software developers to test on various hardware platforms
- **hacked** to do architecture research
- **not** cycle-accurate
  - by default, 1 instruction == 1 cycle
  - we will add use a Simics plug-in to **stall** on memory **misses**
- Simulate memory hierarchy using Simics
Simics

Simics > terminal via ssh

Target# machine terminal via ssh and XWindows

your computer

ssh -Y

t7400-* server (Host)

Simics

Target Machine

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Lab 2 Open-ended Questions

- Study the effect of virtual vs. physical tagging/indexing
- Analyze differences in memory traffic with different cache replacement policies
- Analyze differences in memory traffic for different write-back schemes
- Design a memory hierarchy to make a specific benchmark go fast
- Tune a benchmark to go fast given a memory hierarchy
Memory Hierarchies
Direct Mapped Cache
Direct Mapped Cache

32-k-b  k  b

Input Address

Tag  Index

Tag Decoder  Data Decoder

Valid Bit  MUX

Comparator  Valid Output Driver

2^k entries
4-way Set-associative Cache

32-k-b

Tag Decoder

Data Decoder

2^k entries per way

2^b: cache line size (bytes)
4-way Set-associative Cache

What if, for legacy reasons, the tag size was fixed....

but you got more transistors for the next version of your cache.

What would you do?
How to handle a TLB fill
Example Machine: MIPS R10k

- 0.35 micron process
- 16.6 x 17.9 mm chip
- 298 mm²
- 6.8 million transistors
  - 4.4 million cache
  - 2.4 million logic
- Full-custom design for datapaths and control logic
- Semi-custom design for less critical control logic

Jan 1996 (150-200 MHz) $3,000 for 200 MHz
1997 -> 250nm @ 250 MHz

MIPS R10k: Memory Hierarchy


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MIPS R10k: Memory Hierarchy


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MIPS R10k: Memory Hierarchy

Main Memory

Instr. Cache

Way 0 16Kbyte

Way 1 16Kbyte

virtual indexed

physical tagged

4 Instruction words

Inst Fetch Virtual Address (PC)

Main TLB

Refill

64 entries

Instr TLB

Physical Address

8 entries

Questions?