CS 152
Computer Architecture and Engineering
Lecture 25 -- Digital Imaging

2014-4-24
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(not a prof - “John” is always OK)
TA: Eric Love

www-inst.eecs.berkeley.edu/~cs152/
CMOS imagers sensors are everywhere

2011
2.1B units
5.8B US $

2016 (F)
4B units
10.8B US $

Humans on earth: 6.9B

Year (F == forecast)

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<th>Sales</th>
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<tr>
<td>2014</td>
<td>149</td>
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<tr>
<td>2015</td>
<td>138</td>
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Source: www.icinsights.com
iPhone 5
4.5 x 3.4 mm sensor.

Wednesday, April 23, 14
Canon 5D Mark III
36 x 24 mm sensor.
Wednesday, April 23, 14
Six generations of iPhone camera
Cameras:
9% of the $199 Bill of Materials (BOM).

<table>
<thead>
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<th>Components / Hardware Elements</th>
<th>iPhone 5 Hardware Comments</th>
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<tr>
<td>Camera(s)</td>
<td>8MP + 1.2MP</td>
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<td>$18.00</td>
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Source: IHS iSuppli Research, September 2012

Sony rear camera module

Omnivision camera
2006: 1 year before iPhone
Motorola Q Smart Phone

Moto predicted 3M shipped Q4 2006.

Source: www.elecdesign.com
Camera module cost: $7

4.4% of $158 BOM.

CMOS Camera Sensor
Source: iSuppli Corp. July 2006
Typical camera module for the Micron MT9M111

Fixed-focus lens.
No “optical” zoom.

0.27 inches deep.
0.37 inch x 0.37 inch square

Source: www.asia-optical.com.tw
Micron MT9M111* - 1.3 MPixel CMOS Imager

1280 x 1024 pixels.

Each pixel is R, G, or B.
So, 2/3 of RGB image data is interpolated.

* Photo a close relative (MT9M011)
Camera interface to the outside world

**Simple Power Hookup**

- **8-bit D_{out} Port**
- **54 MHz Clk**
- **1280 x 1024 @ 15 fps**
- **640 x 512 @ 30 fps**
- **YCrCb 4:2:2**

**Serial port to control the camera.**

**Figure 4: 44-Ball iCSP Assignment**

Top View
(Ball Down)
**Sensor Core**
- 1316H x 1048V including black
- 1/3-inch optical format
- Auto black compensation
- Programmable analog gain
- Programmable exposure
- Dual 10-bit ADCs
- Low-power preview mode
- H/W context switch to/from preview
- Bayer RGB output

**Image Flow Processor**
- Camera Control
  - Auto exposure
  - Auto white balance
  - Flicker detect/avoid
  - Camera control: snapshots, flash, video, clip

**Image Flow Processor**
- Colorpipe
  - Lens shading correction
  - Color interpolation
  - Filtered resize and zoom
  - Defect correction
  - Color correction
  - Gamma correction
  - Color conversion + formatting
  - Output FIFO

**SRAM Line Buffers**

**Control Bus**
(Two-Wire Serial I/F Transactions) + Sensor control (gains, shutter, etc.)
Focusing the Camera
Images are inverted on their way to the retina at the back of the eye.
Variable focus

Distant object

Relaxed muscle
Taut ligaments

Near object

Contracted muscle
Slack ligaments
Out of focus
Fixed focus camera module.

Camera Module Exploded View
Fixed-focus: What do we give up?

Camera is only in focus for objects within the depth of field: other objects are blurry.

However, we can set the “far” boundary to “infinity”. Fixed-focus cameras do.
Best we can do with a fixed-focus camera.
Auto-Focus Module in iPhone 5

“Voice Coil” solenoid moves lens element.

Works like a loudspeaker ...

Permanent magnet
Coil
Electrical signals
Dust cap
Inner suspension (spider)
Outer suspension (surround)
Cone
Cone vibrates
High quality images require the use of autofocus functionality in cameras. Changes in distance between the subject and the camera, as well as changes in temperature can cause the image to become blurry and lose its sharpness. An autofocus mechanism enables the recovery of image sharpness by adjusting the position of the optical elements in the camera.

DigitalOptics Corporation™ (DOC) OptiML autofocus (AF) module uses proprietary MEMS actuators to move a lens element inside the camera module for image focusing, while enabling lower profile camera module. The MEMS AF actuator utilizes electrostatic forces to precisely move the lens element with high repeatability, speed, and without any noise. The ultra-low power consumption characteristic of the MEMS actuator enables unique imaging features, such as continuous AF for video without the side effect of generating heat which degrades the imager performance. In addition, the unique mechanical interfaces built into the AF module provide precision optics alignment resulting in the highest image quality.

**OptiML™ MEMS Autofocus Module Features**

- Fits compact camera module design — 6.5 mm x 6.5 mm x < 6.0 mm
- Enables single lens motion AF for high optical MTF — Support image resolution
- Centered optical aperture for centered optics — Large clear aperture supports 1/4” and 1/3” optical formats
- Low Power Consumption (AF only) — Low operating voltage (2.8 to 4.5 V) — Zero power consumption at the infinity position to hold focus in any orientation — Low peak current (7 µA peak) and low power (0.25 mW maximum) to change focus position
- Superior lens positioning performance — Positioning repeatability: ± 3 µm — Hysteresis performance: ± 3 µm — Built-in high precision position sensor for autofocus calibration — Fast settling time: (15ms max)
- Uses MEMS Technology — Long lifetime: 10,000,000 cycles or more — High shock tolerance: 10,000 g — Temperature Range: -20º to 70º C
- Reflow compatible

**Advantages**

- Single lens motion inside the lens barrel — Enables lower profile camera module — Enables larger optical TTL design for better image quality — Enables faster AF due to reduced range of motion and lower mass
- Lens barrel as housing — Enables meeting x-y size specification — Reduces number of parts — Improves alignment of optics to imager — Reduces number of particles on the imager window
- MEMS electrostatic actuation integrated with MEMS motion control — Improves lens alignment and movement precision — Reduces size — Reduces power consumption — Reduces assembly complexity and cost — Integrated capacitive position sensing available

DigitalOptics’ MEMS AF technology can be used in smart phones, digital still cameras, portable computers, toys and other compact electronic devices.

Contact a DOC sales representative for more information.

3025 Orchard Parkway | San Jose, CA 95134 | T +1.704.887.3154 | www.doc.com

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**OptiML AF Module Specifications**

- Module Height: 1.05mm
- Module Diameter: 5.52mm
- Optical Format: 1/4" or 1/3"
- Aperture Diameter: 2.36mm

**Example of a camera module with integrated MEMS AF**

The actuator is integrated inside the camera lens barrel, which reduces the overall height of the camera module.

**Coming soon: MEMS auto-focus**

![MEMS Autofocus Module](image)
Silicon Photosensitivity
Zooming in on the array ...

One Pixel

Pixel Photosensor
Each sensor is a photodiode

Side view:

Top view:
Photodiode: Like a normal diode ...

Quadrant for photosensing.

"Dark current"
When no photons are present.
Photodiodes see a gray world ...

Data shown is for a standard 0.35μ CMOS logic process.

Quantum efficiency can be improved by modifying the process.

42% of photons that fall on the photodiode are converted to electrons (“quantum efficiency”)

Color
Color filters deposited on pixel array

"RGB Bayer"

Why?

Source: Eric Fossum, IEEE Micro, and Micron Data Sheets
Human cone array, imaged through the eye.

Micron MT9M111 spectral response ...

Note IR response. This is why camera module needs an IR filter.
Array border cells aid calibration ...

8 Black Rows

1 Black Column

SXGA (1,280 x 1,024) + 4-pixel boundary for color correction + additional active column + additional active row = 1,289 x 1,033 active pixels

(0, 0)

26 Black Columns

7 Black Rows

(1315, 1047)

Black pixels have photodiodes covered by metal.
Microlenses
Recall: Side view of a photodiode ...

Photons that reflect off metal shielding are lost.

If there was a way to sense the photons that bounce off the metal, low-light photos would look better.
“Compound eyes” of an insect - “microlenses”
Source: http://micro.magnet.fsu.edu/
Pixel Scaling
CMOS Image Sensors: State-Of-The-Art and Future Perspectives

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Abstract
—Over the last decade, CMOS image sensor technology made huge progress. Not only the performance of the imagers was drastically improved, but also their commercial success boomed after the introduction of mobile phones with an on-board camera. Many scientists and marketing specialists predicted 15 years ago that CMOS image sensors were going to completely take over from CCD imagers, in the same way as CCD imagers did mid eighties when they took over the imaging business from tubes [1]. Although CMOS has a strong position in imaging today, it did not rule out the business of CCDs. On the other hand, the CMOS-push drastically increased the overall imaging market due to the fact that CMOS image sensors created new application areas and they boosted the performance of CCD imagers as well.

This paper describes the state-of-the-art of CMOS image sensors as well as the future perspectives.

I. IMPACT OF CMOS SCALING ON IMAGE SENSORS

It is common knowledge that the scaling effects in CMOS technology allow the semiconductor industry to make smaller devices. This rule holds for CMOS imaging applications as well.

Figure 1 gives an overview of CMOS imager data published at IEDM and ISSCC of the last 15 years [2]. The bottom curve illustrates the CMOS scaling effects over the years, as described by the ITRS roadmap [3]. The second curve shows the technology node used to fabricate the reported CMOS image sensors, and the third curve illustrates the pixel size of the same devices.

- CMOS image sensors use a technology node that is lagging behind the technology nodes of the ITRS. The reason for this is quite simple: very advanced CMOS processes used to fabricate digital circuits, are not imaging friendly (issues with large leakage current, low light sensitivity, noise performance, optical issues, …). Compared to the ITRS roadmap, the difference in technology used for image sensors and advanced logic processes is about 3 technology generations,

- CMOS image sensor technology scales almost at the same pace as standard digital CMOS processes do,

- Pixel dimension scales with the technology node used, and the ratio is about a factor of 20.

The MegaPixel race ...

Figure 1. Evolution of pixel size, CMOS technology node used to fabricate the devices and the minimum feature size of the most advanced CMOS logic process.

1-4244-1124-6/07/$25.00 ©2007 IEEE.
Resolution limit of lens technology ...

![Graph showing Airy Disk Diameter and lens resolution vs. wavelength](https://via.placeholder.com/150)

- **Airy Disk Diameter**
  \[ D = 2.44 \lambda \cdot F\# \]

- **Cheap Lens Resolution**
  \( (30 \text{ lp/mm}) \)

- **High Performance Lens Resolution**
  \( (120 \text{ lp/mm}) \)

- **LENS**
  - **F/2.8**
  - **F/11**

- **BGR**

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Weekday, April 23, 14
Why more pixels are not always better

5μm pixels match the optical resolving power of practical camera optical systems (1997, Fossum). 2012 figure may be smaller.

Shrinking pixels beyond limit does not add resolution.

Larger die sizes are the path to higher resolution.
Sensor size: Pro camera vs iPhone 5

Canon 5D Mark III 36 x 24 mm sensor.

35mm full-frame

APS-H

APS-C

1/3-inch
iPhone 5 (approx.)
Megapixels: Benefits other than resolution

Small pixels supersample color space. Color interpolation improves.

Process scaling helps imager arrays in another way ...
Recall: Photodiode design ...

As process shrinks, readout circuits shrink and diode grows. So, fill factor increases and fewer photons lost.
Readout Circuits
Step 1: Fill $C_d$, and sense column current.

Edge circuitry samples current $I(Q_f)$ for later use.

Parasitic photodiode capacitance.
Opening the electronic shutter ...

Step 2: “Electronic shutter” opens, photodiode empties $C_d$.

$Q_d(t)$

$Q_f - \int Q_d(t)$

$C_d$

Too much $\int Q_d(t)$, and we empty bucket before shutter closes.

Not enough $\int Q_d(t)$, and we capture temporal noise.

Limits dynamic range and signal-to-noise.
Close shutter, read pixel value ...

Step 3: Sense how empty $C_d$ has become.

\[ Q_f - \int Q_d(t) \]

Use $I(Q_f)$ from start of the cycle to reduce $kTC$ (reset) noise.

"Correlated double sampling"

Temporal noise affects $Q_f$ value.
This ever-present photon shot noise component has a very interesting impact on the signal-to-noise behavior of an imaging system: in the case of a perfect noise-free imager in a perfect noise-free camera, the performance of the camera system is fully photon-shot-noise limited. The maximum signal-to-noise ratio (S/N)\text{MAX} is then given by:

\[
\text{S/N}_{\text{MAX}} = \sqrt{\frac{e}{N}} = \sqrt{\frac{1}{10,000}}
\]

or, the maximum signal-to-noise ratio is equal to the square root out of the signal value! This observation leads to an interesting rule of thumb: to make decent images for consumer applications, a minimum signal-to-noise ratio of 40 dB or more is needed, translated by means of the abovementioned formula into 10,000 electrons within every pixel. (This number tends to slowly go down due to extensive image processing and image-noise removal.)

On one hand, while the CMOS technology is shrinking further down, allowing for smaller pixels, the lower limit of the pixel size will no longer be determined by the minimum dimensions set by the CMOS technology, but it will be determined by the amount of electrons that can be stored in the pixel.

IV. ANALOG-TO-DIGITAL CONVERTERS FOR CMOS IMAGE SENSORS

It should be clear that in the era of digital imaging, most CMOS image sensors are provided with an analog-to-digital converter allowing the output signal to be accessible in the digital domain. Classical ADC architectures can be used in combination with the CMOS imager, e.g. flash converter, sigma-delta converter, successive approximation, single-slope ADC, pipelined ADC, cyclic ADC, etc. Only one particular architecture will be discussed in this paper: the single-slope ADC. This concept is very appealing in the case the CMOS imager is provided with an ADC for every column or even for every pixel. Especially column-parallel conversion has some very interesting advantages for high-speed applications. Because in this case the sensor chip has as many ADCs as it has columns, and all these ADCs work fully in parallel [11].

The basic working principle of the single-slope ADC is illustrated in Figure 7. The analog input signal \( \text{V}_{\text{IN}} \) that needs to be converted, is compared to an analog ramp signal \( \text{V}_{\text{ramp}} \). A digital counter generates the latter. At the moment that the two voltages \( \text{V}_{\text{IN}} \) and \( \text{V}_{\text{ramp}} \) are equal to each other, the comparator changes state and latches the counter value into a memory. The data stored into the memory will be the digital value corresponding to the analog input voltage \( \text{V}_{\text{IN}} \).

In the case of column-parallel conversion, the imager has at every column a comparator and a digital memory. The digital counter is common for all pixels on a single row.

After digitization, the output signal of the camera will have an extra quantization noise component equal to:

\[
12\text{LSB} = \frac{\text{V}_{\text{LSB}}}{\text{ADC}}
\]

with \( \text{V}_{\text{LSB}} \) being the analog voltage of the least significant bit.

In relation to the photon shot noise, an interesting observation can be made: the noise floor in the output signal of an image sensor is always (best-case) determined by the photon shot noise. The latter will be small for small output signals of the sensor, but it will be large for large output signals of the sensor. In the case of a large output signal, the quantization error of the ADC does not have to be as low as it should be for smaller output signals. This idea allows an ADC converter with an adaptive quantization step: small for small signals, large for large signals. This idea can be relatively easily implemented by means of the single-slope ADC. In that case the ramp, generated originally by the digital counter, will be no longer linear with...
Camera Shutter: Space-Time Sampling

Rolling Shutter (CMOS) vs. Global Shutter (CCD)
Global shutter.
Fan in motion.
Rolling shutter.
Solution: Add “analog memory” ...

Does not come for free.

Reduces fill factor, adds edge circuit complexity.

Mechanical shutters are more popular.
AWARE-2: Array of 98 phone camera modules (14 M-pixel)

1.3 G-pixel camera @ 3 frames/sec
Tone mapping creates an individual 32-bit/8-bit conversion for each pixel in the scene, but ensures that the mappings vary smoothly from pixel to pixel. The majority of the display dynamic range is used on shadows and highlights, with mid-tones compressed. The tone-mapped image more accurately matches human visual processing because our vision is foveated and our pupils adjust as we examine different regions of a wide field. More details on the compositing process are provided in Supplementary Information.

The maximum pixel count for an imager with aperture diameter $A$ and the mean operating wavelength $\lambda$ is $S = \frac{5}{A^2} \sin^2(\text{FOV}/2)/\lambda^2$ (ref. 2). For AWARE-2, FOV $= 120'\mu$ and $A = 16$ mm, corresponding to a limit of two gigapixels at an operating wavelength of 550 nm. At its design capacity of 220 microcameras, a fully populated AWARE-2 would capture three gigapixels but the estimated field would decrease to two gigapixels after sensor regions with limited illumination had been removed and overlapping regions had been merged. AWARE-2’s resolution is illustrated by the star field shown in Fig. 4, which shows details of a gigapixel sky survey with an exposure time of 1.85 s. Faint stars in this image illuminate two to four pixels after median filtering to remove hot pixels and logarithmic intensity mapping to fill the display dynamic range. We anticipate that higher-resolution multiscale systems with terrestrial motion compensation and microcamera adaptive optics to remove atmospheric blur may be developed for space situational awareness.

As shown in systematic resolution images and modulation transfer function measurements presented in Supplementary Information, section 4b, most of the blur in the star field image is due to defects in AWARE-2’s microcamera lenses. To allow low-cost gigapixel array integration, AWARE-2 uses injection-moulded plastic relay optics. These lenses may be moulded with aspheric surfaces, requiring fewer elements and consequently less volume and mass than a spherical glass-element camera with similar performance. However, birefringence in the fabricated optics due to residual stresses introduced during moulding degrades AWARE-2’s image quality and resolution relative to fundamental limits. We expect newer high-index plastics that minimize birefringence to enable the camera to approach these theoretical limits.

We have also built glass microcamera lenses and, as shown in Supplementary Information, section 4c, AWARE-2 achieves pixel-limited optical resolution with these lenses.

Figure 1 | Pungo Lake as captured using AWARE-2. The total FOV is 120' by 50' and the composite image here consists of 0.96 gigapixels, where each pixel has an instantaneous FOV of 38' m. The measured values are logarithmically mapped to make better use of the display dynamic range. The relative responsivities of the individual microcameras were adjusted iteratively to minimize variation across sub-image boundaries. The labelled regions are referred to in Fig. 2.

Figure 2 | Details of Fig. 1. a–e, Labelled regions in Fig. 1. The swans in c are 114 pixels long and are 310–350 m from AWARE-2. Each pixel corresponds to 13 mm at the position of the swans. In d, the most distant bird is 17 pixels long and the closest is 70 pixels long. The limited depth of focus of the camera is illustrated in e, where regions of the foreground foliage are in sharpest focus.
Figure 2

(a) Original images of the swans. (b) AWARE-2's reconstruction of the scene, with the original image overlaid. (c) Each pixel has an instantaneous FOV of 38 mrad. The measured values are (a) 120 mm, corresponding to the position of the swans. In (b) the closest bird is 70 mm long and are 310–350 m from AWARE-2. Each pixel corresponds to 13 mm at the position of the swans. In (c) the most distant bird is 17 mm long. The limited depth of focus of the camera is fundamental limits. We expect newer high-index plastics that minimize imaging degrades AWARE-2's image quality and resolution relative to fun-

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Let x, y be the x, y position of a pixel, let f(x, y) be the function to be mapped image more accurately matches human visual processing on shadows and highlights, with mid-tones compressed. The tone-mapping process are provided in Supplementary Information.

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Let x, y be the x, y position of a pixel, let f(x, y) be the function to be mapped image more accurately matches human visual processing on shadows and highlights, with mid-tones compressed. The tone-mapping process are provided in Supplementary Information.
AWARE-2 demonstrates that the age of ever-increasing pixel count is far from over. Although development of high-performance, low-cost microcamera optics and optomechanics have been the main challenge in the present stage of multiscale camera development, integrated circuits, rather than optics, remain the primary barrier to ubiquitous high-pixel-count imaging. To accommodate the electronics and allow for heat dissipation (the camera expends 430 W during image acquisition), AWARE-2 is mounted in a 0.75 m$^3$ frame. The optical system occupies less than 3% of the system volume. The size of the camera is dictated both by the size of the electronic control boards and the need to cool them effectively. As more efficient and compact electronics are developed, hand-held gigapixel photography may become an everyday reality.

Figure 3 | Traffic circle captured using AWARE-2. Insets are digitally magnified by a factor of 13. Distances to the inset regions range from 15 m ('no parking' sign; first from left) to 92 m (detail of building; third from left). The exposure time for each microcamera was set independently of the others, and a tone-mapping algorithm was used to convert the resulting HDR image for display. Global distortion associated with mapping the 120$^\circ$ horizontal field onto a flat image is apparent.

Figure 4 | Details of a star field captured using AWARE-2 with a 1.85-s exposure time. Image data was logarithmically mapped to display values to make better use of the available display dynamic range. Stars with apparent magnitudes of $m = 8.2$ mag are visible in the image. However, those with $m \leq 3.5$ mag saturate the detector at this exposure time.
Break
Fabrication Technology
Better to replace poly MOSFET photogate with JFET photogate (a.k.a. pinned photodiode or buried photodiode)

First demonstrated by JPL/Kodak collaboration in 1995

Lee, Gee, Guidash, Lee and Fossum 1995 IEEE CCD AIS Workshop
Pixel Sharing – Examples of 1.4 µm Pixels

2T and 1.75T effective transistors per pixel.

1.75 effective transistors per pixel.
The fundamental motivations for the imaging industry to pursue Moore's Law type of scaling are comparable to that of the broader semiconductor industry. Additionally, advancements within advanced technology nodes manufacturing have resulted in advanced processes. The motivations for the imaging industry to pursue Moore's Law type of scaling are comparable to that of the broader semiconductor industry. Additionally, advancements within advanced technology nodes manufacturing have resulted in advanced processes.

Advanced Materials

A. Background of CMOS Image Sensor Pixels

Chipworks has obtained charge-coupled devices (CCD) and Image Sensor Technologies (CIS) chips from leading manufacturers and performed structural, compositional, and design analyses to benchmark the technology of the market leaders. Of these technology sectors, image sensor manufacturers have realized many benefits from innovation by the leaders.

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Front Illuminated CIS – BEOL Stack Thinning

2.0 µm green filter

2.2 µm red filter

Optical stack thinning continues

Innovative color filter cavity fill process
Neighboring photocathodes isolated using oxide filled deep trench isolation (DTI)

Photocathode region
Front-illuminated system-on-chip (SoC) CIS devices require substantial substrate engineering.

- **P-type substrate**
  - N-well in P-epi layer
  - Pixel array P-well
  - N-type photocathodes

- **N-type substrate**
  - Pixel array P-well
  - N-epi
  - Highly doped NBL

N-type substrates are used for n-type photocathodes.
65 nm design rules enable large diameter light pipes.
Fig. 6 shows examples of the Sony and OmniVision first generation BI devices. Sony’s device was fabricated using a silicon-on-insulator (SOI) process, in which a conventional CMOS process flow was run on SOI wafers with 3 µm thick active silicon. After completion of the FEOL and BEOL structures, the planarized dielectric stack served as a bonding surface for the joining of the SOI wafer to a silicon chip carrier wafer using an adhesive bonding technique. Next, the sacrificial SOI handle wafer and buried (BOX) layers were removed. The unobstructed back of the substrate functions as the light receiving surface.

For many FI devices, the reflectivity of planar silicon had been addressed through the use of silicon nitride films deposited over the photocathode regions to serve as anti-reflection (AR) layers. For its first BI device, Sony chose to use a hafnium oxide (HfO$_2$) AR layer blanket deposited over the back of the die. It also included tungsten metallization on the back which optically shielded the peripheral regions, and was patterned to form an aperture grid improving color separation in the pixel array.

While Sony’s device had a 1.77 µm pixel size and relatively large form factor module for camcorder applications, OmniVision’s first BI device featured a 1.4 µm pixel size, and was deployed in a small form factor camera module. OmniVision and TSMC developed a bulk BI process for their 1.4 µm pixel size sensor, fabricated using 0.11 µm generation process technology [6, 7]. The device used oxide bonding to join the planarized finished wafer to a silicon carrier wafer. The bulk P-type substrate with P-epitaxial layer was mechanically back ground and wet etched, with the epi serving as an etch stop. The resulting substrate thickness was 2.1 µm and displayed some back surface roughness, an artifact of the wafer thinning process. A back surface implant and laser anneal process were used to reduce the crystal defects induced by the wafer thinning process. Due to the small form factor application, OmniVision also adapted its wafer level chip scale (WL-CSP) packaging, first used for its FI devices, to the new BI device structure.
Back-Side Illumination
We are developing monolithic pixel devices utilizing a monolithic SOI technology provided by OKI Semiconductor Co., Ltd. Fig. 1 illustrates schematics of our SOI pixel device. By using bonded wafers, we adopt a high resistivity (approximately 400 \text{ \textmu } \text{cm}) Czochralski grown substrate for full depletion, which is necessary for front illumination. Thinning is mandatory in our structures may occupy the substantial area reducing the area required in back illumination. In photo-imaging applications, back illumination is desirable to enhance the photo sensitivity [2], [3]. This is particularly important for pixels with smaller sizes, since the on-pixel signal to noise ratio for traversing charged particle detection.

In high-energy physics experiments, for example, the response to infrared and red lasers injected from the front and backside illumination, which is desirable to enhance the photo sensitivity. The wafer was thinned commercially by DISCO Corp. and realized in this study. There is a window of 5 \text{ \textmu } \text{m} by TAIKO process [7]. We examined the thinning process induced damage through the leakage current. Small increase in the leakage current was obtained, demonstrating excellent performance to infrared and red laser lights was obtained, demonstrating the thinning process. Excellent performance to infrared and red laser lights was obtained, demonstrating the thinning process.

For the thinning procedure, the wafer was thinned to 100 \text{ \textmu } \text{m} square where there is no metal layers at the center, allowing front illumination. In our standard procedure, the backside is processed, are separated by a 200 nm thick buried oxide (BOX) layer. In our standard procedure, the backside is processed, are separated by a 200 nm thick buried oxide (BOX) layer. The SOI fabrication was carried out on a basis of multi-project wafer runs, processing various types of sensors on a 8\" wafer. We picked up INTPIX3b chips [4] in order to investigate the thinning quality. The INTPIX3 is a first device where BPW's are integrated. The INTPIX3b chip is a signal evaluation to 128 pixels of 0.2 \text{ \textmu } \text{m} square. The outer chip size is 5 mm square. Each pixel is divided into eight regions and different configurations are divided into eight regions and different configurations are divided into eight regions and different configurations are divided into eight regions and different configurations are divided into eight regions and different configurations are divided into eight regions and different configurations are divided into eight regions and different configurations are divided into eight regions and different configurations are divided into eight regions.

In order to optimize the BPW configuration, the pixels are connected to the SOI MOS contact (Bias Ring). The latter is necessary for front illumination. For the thinning procedure, the wafer was thinned to 100 \text{ \textmu } \text{m} square where there is no metal layers at the center, allowing front illumination. The INTPIX3 is a first device where BPW's are integrated. The INTPIX3b chip is a signal evaluation to 128 pixels of 0.2 \text{ \textmu } \text{m} square. The outer chip size is 5 mm square. Each pixel is divided into eight regions and different configurations are divided into eight regions and different configurations are divided into eight regions and different configurations are divided into eight regions and different configurations are divided into eight regions and different configurations are divided into eight regions and different configurations are divided into eight regions and different configurations are divided into eight regions and different configurations are divided into eight regions and different configurations are divided into eight regions and different configurations are divided into eight regions and different configurations are divided into eight regions and different configurations are divided into eight regions and different configurations are divided into eight regions and different configurations are divided into eight regions and different configurations are divided into eight regions and different configurations are divided into eight regions and different configurations are divided into eight regions and different configurations are divided into eight regions and different configurations are divided into eight regions and different configurations are divided into eight regions and different configurations are divided into eight regions and different configurations are divided into eight regions and different configurations are divided into eight regions and different configurations are divided into eight regions and different configurations are divided into eight regions and different configurations are divided into eight regions and different configurations are divided into eight regions and different configurations are divided into eight regions and different configurations are divided into eight regions and different configurations are divided into eight regions and different configurations are divided into eight regions and different configurations are divided into eight regions and different configurations are divided into eight regions and different configurations are divided into eight regions and different configurations are divided into eight regions and different configurations are divided into eight regions and different configurations are divided into eight regions and different configurations are divided into eight regions and different configurations are divided into eight regions and different configurations are divided into eight regions and different configurations are divided into eight regions and different configurations are divided into eight regions and different configurations are divided into eight regions and different configurations are divided into eight regions and different configurations are divided into eight regions and different configurations are divided into eight regions and different configurations are divided into eight regions and different configurations are divided into eight regions and different configurations are divided into eight regions and different configurations are divided into eight regions and different configurations are divided into eight regions and different configurations are divided into eight regions and different configurations are divided into eight regions and different configurations are divided into eight regions and different configurations are divided into eight regions and different configurations are divided into eight regions and different configurations are divided into eight regions and different configurations are divided into eight regions and different configurations are divided into eight regions and different configurations are divided into eight regions and different configurations are divided into eight regions and different configurations are divided into eight regions and different configurations are divided into eight regions and different configurations are divided into eight regions and different configurations are divided into eight regions and different configurations are divided into eight regions and different configurations are divided into eight regions and different configurations are divided into eight regions and different configurations are divided into eight regions and different configurations are divided into eight regions and different configurations are divided into eight regions.
Fig. 6 shows examples of the Sony and OmniVision first generation BI devices. Sony's device was fabricated using a silicon-on-insulator (SOI) process, in which a conventional CMOS process flow was run on SOI wafers with 3 µm thick active silicon. After completion of the FEOL and BEOL structures, the planarized dielectric stack served as a bonding surface for the joining of the SOI wafer to a silicon chip carrier wafer using an adhesive bonding technique. Next, the sacrificial SOI handle wafer and buried (BOX) layers were removed. The unobstructed back of the substrate functions as the light receiving surface.

For many FI devices, the reflectivity of planar silicon had been addressed through the use of silicon nitride films deposited over the photocathode regions to serve as anti-reflection (AR) layers. For its first BI device, Sony chose to use a hafnium oxide (HfO$_2$) AR layer blanket deposited over the back of the die. It also included tungsten metallization on the back which optically shielded the peripheral regions, and was patterned to form an aperture grid improving color separation in the pixel array.

While Sony's device had a 1.77 µm pixel size and relatively large form factor module for camcorder applications, OmniVision's first BI device featured a 1.4 µm pixel size, and was deployed in a small form factor camera module. OmniVision and TSMC developed a bulk BI process for their 1.4 µm pixel size sensor, fabricated using 0.11 µm generation process technology [6, 7]. The device used oxide bonding to join the planarized finished wafer to a silicon carrier wafer. The bulk P-type substrate with P-epitaxial layer was mechanically back ground and wet etched, with the epi serving as an etch stop. The resulting substrate thickness was 2.1 µm and displayed some back surface roughness, an artifact of the wafer thinning process. A back surface implant and laser anneal process were used to reduce the crystal defects induced by the wafer thinning process. Due to the small form factor application, OmniVision also adapted its wafer level chip scale (WL-CSP) packaging, first used for its FI devices, to the new BI device structure.
A range of substrate thicknesses (2.1 µm to 4.0 µm) has been observed for production 1.4 µm pixel BSI devices.

Transfer gate

N-photocathode

Isolation

P-well

P-type passivation implant
2.0 effective transistors per pixel.
10.3MPixel
1.65 x 1.65 μm²

Figure 22.9.1: Schematic diagram and basic timing.
Figure 22.9.2: 1.65µm pixel cross-section.
Figure 22.9.3: Measured spectrum.
Figure 22.9.4: Optical angle response.
Figure 22.9.5: Specification and characteristics.
Figure 22.9.6: Reproduced image (F2.8, D55, 50fps, Tint20ms, Gain32x).
Si carrier wafer

Al bond pad

bond pad window

wafer bond

thin Si image sensor substrate

Au ball bond
Wafer-Scale Packaging
Fixed focus camera module.

Camera Module Exploded View
OmniVision’s VGA wafer-level camera

Wafer-level cameras

In order to manufacture low-cost camera modules, the main cost drivers — the image sensor, the optical module and the fixture used to assemble the module to the phone board — have to be reduced to a strict minimum.

The image sensors lend themselves rather well to low-cost manufacturing due to their wafer-level manufacturing approach. With this approach it is possible to manufacture optical lenses at the wafer-level, thus creating a very low-cost wafer-level optical module (or wafer-level optics). Another benefit of WLOptics is their flow-compatible materials. By eliminating the plastic lenses used in standard optical modules, the camera modules become compatible with flow soldering, and thus can be integrated at the same time as the other surface mount components on the phone board.

One way to optimize this flow compatibility is to package the image sensor at the wafer-level by redistributing the pads to the back side. This also reduces the camera module area to the image sensor area.

OmniVision CameraCube

A pioneer of the CMOS Image Sensor industry, OmniVision released its latest wafer level camera, the OVM7692, in 2010.

The OVM7692 is a VGA flowable camera module which integrates a Wafer-Level Packaged CMOS Image Sensor and Wafer-Level Optics. The camera module is provided in a 2.8 x 3.2 x 2.5 mm 25-pin package, and integrates a 1.75—m pixel CMOS Image Sensor (CIS), ref. OV289AA from OmniVision, which is manufactured by TSMC using a CMOS technology with a 0.11—m process.

Wafer-level optics

The wafer-level optical module of the OVM7692 is currently outsourced to VisEra Technologies in Taiwan. VisEra was founded in December 2003 as a joint venture between TSMC and OmniVision. On June 30, 2011, OmniVision paid $45M for VisEra’s WLOptics manufacturing operations, and expects to close the transaction in the second quarter of 2012. According to OmniVision, this transaction will allow for streamlining the production process, consolidating the supply chain, expanding the production capacity and reducing the cost.

Whether it’s for the main camera of low-cost phones or the front-facing camera of high-end phones, low-cost, low-resolution camera modules are extremely important.

OmniVision OVM7692 CameraCubeChip™

(Courtesy of System Plus Consulting)

OmniVision OVM7692 cross-section

(Courtesy of System Plus Consulting)

Glass wafer #1 with IR filter

Glass wafer #2 with lens #1 and aperture

Glass wafer #3 (Spacer)

Glass wafer #4 with lens #2

Glass wafer #5 (Carrier wafer)

CIS

Solder ball

OmniVision OVM7692 cross-section
(Courtesy of System Plus Consulting)
Nemotek wafer-level camera

The reflow compatibilities of WLCs provide a big advantage over traditional camera modules, since they can partake in the same reflow soldering process used for assembling the other electronic components on a board.

Nemotek Technologie

Founded in 2008, Nemotek Technologie manufactures customized WLCs for portable applications. Nemotek provides design, manufacturing and testing services for WLCs, as well as for Wafer-Level Packaging (WLP) and Wafer-Level Optics (WLO).

Nemotek's Wafer-Level Packaging and Wafer-Level Optics products use technologies licensed by Tessera.

Nemotek operates a 12,000m² facility in Morocco, including a Class 10 clean room.

Wafer-level camera

The camera is a fixed-focus VGA module integrating a Wafer-Level Packaged CMOS Image Sensor and Wafer-Level Optics. The camera module is provided in a 3.7x3.3x2.4mm 21-pin package, compatible with reflow soldering.

The WLP CIS die and the WL-Optics die are integrated at the die-level using die attach. The final stack is encapsulated into an epoxy resin.

Wafer-Level Packaging

The Wafer-Level Packaging is based on Tessera's Shellcase® MVP solution. The Shellcase process was used in the previous Wafer-Level Camera we analyzed (the Omnivision OVM7692), but it employed a redistribution of the CIS pads to the back side through the edge of the die, using a "T-contact" (Tessera Shellcase RT process). This time, redistribution is realized using Through-Silicon Vias (TSVs) to connect the bond pads of the die and the BGA interface on the rear face of the package.

The TSV manufacturing process used is very different from the typical TSV process, since tapered holes are etched into the Silicon wafer, as opposed to high aspect ratio holes. Therefore, the holes are made with low-cost/high-throughput equipment, instead of expensive DRIE equipment.

In the same fashion, the TSVs are insulated with a thick, low-cost polymer deposited by electrophoretic deposition process, instead of thin Silicon Oxide deposited by PECVD.

The lead used to connect the pads of the CIS with the solder balls consists of an aluminum/copper conductive layer and a nickel/phosphorus plating layer. The lead penetrates through the bond pad to form a circumferential edge contact.

The CIS is protected by a glass carrier, sealed with an epoxy bonding process.

Wafer-level optics

The wafer-level optics is a single wafer element, reflow compatible, based on Tessera's OptiML™ solution.

Two lenses made with a UV curable polymer are manufactured on a borosilicate glass wafer with a replication process. A plastic tool (likely...
The lenses wafer is separated from the image sensor by a FR-4 spacer wafer (Glass-Fiber-Reinforced Plastic). The lenses wafer is sandwiched with layers of Silicon oxide). The package consists of an assembly of four glass wafers.

The lenses are covered with a thin anti-reflective coating. Each master can be used to imprint a large number of lenses. To wrap things up, the complete Wafer-Level Packaging of the CIS camera module results in a significant reduction of the housing costs of electronics components.

Since 2006, Romain is in charge of costing analyses of MEMS devices, costing, and overhead related to multiple subcontractors. It is a "one-stop shop" which provides a complete service.

Romain Fraux is Project Manager for Reverse Costing at System Plus Consulting. He has significant experience in the modeling of the manufacturing costs of electronics boards. He has a BEng from Heriot-Watt University (Edinburgh, Scotland) and a master's degree in Microelectronics from the University of Nantes, France.
evolution of the mobile phone camera

- **OV7660 VGA**
  - Circa 2004
  - 6x6x5mm

- **OV7640 VGA**
  - 8x8x6mm

- **OV7670 VGA**
  - Circa 2005
  - 6x6x4mm

- **OV7680 VGA**
  - Circa 2006
  - 4.5x4.5x3mm

- **OV7690 VGA**
  - 2009
  - 2.5x2.9x2.5mm

- **Reflowable 2 surface lens made at wafer level**

- **Reflowable 1 glass element glued onto CSP**

- 2002
- 2005
- 2008
Camera Modules ...

Design shown is "dominant paradigm".

Evolves with every product generation.

Some research projects and start-ups focus on the evolution.

Others shoot for "revolutionary jump"
On Tuesday

Preparing for the mid-term ...

Have a good weekend!