CS 152 Computer Architecture and Engineering

Lecture 17: Synchronization and Sequential Consistency

Dr. George Michelogiannakis
EECS, University of California at Berkeley
CRD, Lawrence Berkeley National Laboratory

http://inst.eecs.berkeley.edu/~cs152
Administrivia

- PS 4 due NOW

- Quiz 4 Monday April 11th
  - Please be on time

- Lab 4 due in a week (Wednesday April 13th)

- PS 5 is out
Last Time, Lecture 16: GPUs

- Data-Level Parallelism the least flexible but cheapest form of machine parallelism, and matches application demands
- Graphics processing units have developed general-purpose processing capability for use outside of traditional graphics functionality (GP-GPUs)
- SIMT model presents programmer with illusion of many independent threads, but executes them in SIMD style on a vector-like multilane engine.
- Complex control flow handled with hardware to turn branches into mask vectors and stack to remember µthreads on alternate path
- No scalar processor, so µthreads do redundant work, unit-stride loads and stores recovered via hardware memory coalescing
Uniprocessor Performance (SPECint)


- **VAX**: 25%/year 1978 to 1986
- **RISC + x86**: 52%/year 1986 to 2002
- **RISC + x86**: ??%/year 2002 to present

Graph showing performance trends from 1978 to 2006, with 25%/year for VAX 1978 to 1986, 52%/year for RISC + x86 1986 to 2002, and ??%/year for RISC + x86 2002 to present.
Power, Frequency, ILP

Intel CPU Trends
(sources: Intel, Wikipedia, K. Olukotun)

- Dual-Core Itanium 2
- Pentium 4
- Pentium
- 386

- Transistors (000)
- Clock Speed (MHz)
- Power (W)
- Perf/Clock (ILP)
40 years of Semiconductor Scaling History

- Modern CMOS
- Beginning submicron CMOS
- Deep UV litho
- 65 nm in 2006
- 28 nm in 2012
- Presumed limit to scaling

Moore's Law: The rate of progress in the semiconductor industry has been exponential over the past 40 years. However, the rate is slowing down.

Atomic scale limit case for 2D Lithography Scaling

End of Moore's Law: A series of one-offs can never substitute for an exponential growth.

http://www.v3.co.uk/v3-uk/news/2403113/intel-predicts-moores-law-to-last-another-10-years
Intel Adapts To Slowdown

 Yesterday
 PROCESS TECHNOLOGY
 TICK (PROCESS) TOCK (ARCHITECTURE)

 Today
 PROCESS TECHNOLOGY
 PROCESS ARCHITECTURE OPTIMIZATION
Why Power Is No Longer Reducing

- Dennard’s scaling

- Power = activity_factor * C * F * V^2
  - Capacitance is reduced with area (smaller technology)

- Why can’t we scale down voltage any more?
Threshold Voltage

![Graph showing Threshold Voltage](image)

- **Dynamic Energy**
- **Leakage Energy**
- **Total Energy**
Frequency Has Stopped Scaling Too
Parallel Processing

- “We are dedicating all of our future product development to multicore designs. ... This is a sea change in computing”
  – Paul Otellini, President, Intel (2005)

- All microprocessor companies switch to MP (2+ CPUs/2 yrs)
Name MultiCore Systems
Symmetric Multiprocessors

- All memory is equally far away from all processors
- Any processor can do any I/O (set up a DMA transfer)

**Diagram:**
- Processors connected to CPU-Memory bus
- Memory connected to CPU-Memory bus
- I/O controllers connected to I/O bus
  - Graphics output
  - Networks
Why Would We Want Asymmetry?
Synchronization

The need for synchronization arises whenever there are concurrent processes in a system (even in a uniprocessor system)

Two classes of synchronization:

**Producer-Consumer**: A consumer process must wait until the producer process has produced data

**Mutual Exclusion**: Ensure that only one process uses a resource at a given time
A Producer-Consumer Example

The program is written assuming instructions are executed in order.

Producer posting Item \( x \):
- Load \( R_{\text{tail}} \), (tail)
- Store \((R_{\text{tail}}), \, x\)
- \(R_{\text{tail}} = R_{\text{tail}} + 1\)
- Store (tail), \( R_{\text{tail}} \)

Consumer:
- Load \( R_{\text{head}}, \) (head)
- spin:
  - Load \( R_{\text{tail}}, \) (tail)
  - if \( R_{\text{head}} = R_{\text{tail}} \) goto spin
  - Load \( R, \) (\( R_{\text{head}} \))
  - \( R_{\text{head}} = R_{\text{head}} + 1\)
  - Store (head), \( R_{\text{head}} \)
- process\( (R) \)

Problems?
A Producer-Consumer Example continued

Producer posting Item x:

1. Load $R_{\text{tail}}$, (tail)
2. Store $(R_{\text{tail}})$, x
   $R_{\text{tail}} = R_{\text{tail}} + 1$

Consumer:

spin:
1. Load $R_{\text{head}}$, (head)
2. if $R_{\text{head}} == R_{\text{tail}}$ goto spin
3. Load $R$, $(R_{\text{head}})$
   $R_{\text{head}} = R_{\text{head}} + 1$
   Store (head), $R_{\text{head}}$

Can the tail pointer get updated before the item x is stored?

Programmer assumes that if 3 happens after 2, then 4 happens after 1.

Problem sequences are:

2, 3, 4, 1
4, 1, 2, 3
Sequential Consistency

A Memory Model

“A system is \textit{sequentially consistent} if the result of any execution is the same as if the operations of all the processors were executed in some sequential order, and the operations of each individual processor appear in the order specified by the program”

\textit{Leslie Lamport}

Sequential Consistency =

arbitrary \textit{order-preserving interleaving} of memory references of sequential programs
Sequential Consistency

Sequential concurrent tasks: $T_1, T_2$
Shared variables: $X, Y$ (initially $X = 0, Y = 10$)

$T_1$:
- Store $(X), 1 \ (X = 1)$
- Store $(Y), 11 \ (Y = 11)$

$T_2$:
- Load $R_1, (Y)$
- Store $(Y'), R_1 \ (Y' = Y)$
- Load $R_2, (X)$
- Store $(X'), R_2 \ (X' = X)$

what are the legitimate answers for $X'$ and $Y'$ ?

$\{(X', Y') \in \{(1,11), (0,10), (1,10), (0,11)\}$

*If $y$ is 11 then $x$ cannot be 0*
Sequential Consistency

Sequential consistency imposes more memory ordering constraints than those imposed by uniprocessor program dependencies.

What are these in our example?

T1:
- Store (X), 1 (X = 1)
- Store (Y), 11 (Y = 11)

T2:
- Load R₁, (Y)
- Store (Y'), R₁ (Y' = Y)
- Load R₂, (X)
- Store (X'), R₂ (X' = X)

additional SC requirements

Does (can) a system with caches or out-of-order execution capability provide a *sequentially consistent* view of the memory?

*more on this later*
Issues in Implementing Sequential Consistency

Implementation of SC is complicated by two issues

• *Out-of-order execution capability*

  - Load(a); Load(b)  yes
  - Load(a); Store(b) yes if a ≠ b
  - Store(a); Load(b) yes if a ≠ b
  - Store(a); Store(b) yes if a ≠ b

• *Caches*

  Caches can prevent the effect of a store from being seen by other processors

  *No common commercial architecture has a sequentially consistent memory model!*
Memory Fences

Instructions to sequentialize memory accesses

Processors with *relaxed or weak memory models* (i.e., permit Loads and Stores to different addresses to be reordered) need to provide *memory fence* instructions to force the serialization of memory accesses.

Examples of processors with relaxed memory models:
- Sparc V8 (TSO,PSO): Membar
- Sparc V9 (RMO):
  - Membar #LoadLoad, Membar #LoadStore
  - Membar #StoreLoad, Membar #StoreStore
- PowerPC (WO): Sync, EIEIO
- ARM: DMB (Data Memory Barrier)
- X86/64: mfence (Global Memory Barrier)

*Memory fences are expensive operations, however, one pays the cost of serialization only when it is required*
Using Memory Fences

Producer posting Item x:
- Load $R_{tail}$, (tail)
- Store $(R_{tail}), x$
  - Membar_{SS} (tail)
  - $R_{tail} = R_{tail} + 1$
  - Store (tail), $R_{tail}$

Ensures that tail ptr is not updated before x has been stored

Consumer:
- Load $R_{head}$, (head)
- spin:
  - Load $R_{tail}$, (tail)
  - if $R_{head} == R_{tail}$ goto spin
  - Membar_{LL} (tail)
  - Load R, (R_{head})
  - $R_{head} = R_{head} + 1$
  - Store (head), $R_{head}$

Ensures that R is not loaded before x has been stored

Process(R)
Multiple Consumer Example

Producer posting Item x:
- Load $R_{tail}$, (tail)
- Store ($R_{tail}$), x
- $R_{tail} = R_{tail} + 1$
- Store (tail), $R_{tail}$

Consumer:
- Load $R_{head}$, (head)
- spin:
  - Load $R_{tail}$, (tail)
  - if $R_{head} == R_{tail}$ goto spin
  - Load R, ($R_{head}$)
  - $R_{head} = R_{head} + 1$
  - Store (head), $R_{head}$

Critical section:
Needs to be executed atomically by one consumer

What is wrong with this code?
Mutual Exclusion Using Load/Store

A protocol based on two shared variables c1 and c2. Initially, both c1 and c2 are 0 (not busy)

**Process 1**

```
...  
c1=1;
L: if c2=1 then go to L
   < critical section>
c1=0;
```

**Process 2**

```
...  
c2=1;
L: if c1=1 then go to L
   < critical section>
c2=0;
```

What is wrong? **Deadlock!**
Mutual Exclusion: *second attempt*

To avoid *deadlock*, let a process give up the reservation (i.e. Process 1 sets \( c_1 \) to 0) while waiting.

- Deadlock is not possible but with a low probability a *livelock* may occur.

- An unlucky process may never get to enter the critical section \( \Rightarrow \) *starvation*

\[
\begin{align*}
\text{Process 1} & \quad & \text{Process 2} \\
\text{...} & \quad & \text{...} \\
L: & \quad & L: \\
\text{c1=1;} & \quad & \text{c2=1;} \\
\text{if c2=1 then} & \quad & \text{if c1=1 then} \\
\quad & \quad & \quad \\
\{ \text{c1=0; go to L}\} & \quad & \{ \text{c2=0; go to L}\} \\
\text{< critical section>} & \quad & \text{< critical section>} \\
c1=0 & \quad & c2=0
\end{align*}
\]
A Protocol for Mutual Exclusion

T. Dekker, 1966

A protocol based on 3 shared variables c1, c2 and turn. Initially, both c1 and c2 are 0 (not busy)

**Process 1**

```plaintext
...  
c1=1;
turn = 1;
L: if c2=1 & turn=1
    then go to L 
    < critical section>
c1=0;
```

**Process 2**

```plaintext
...  
c2=1;
turn = 2;
L: if c1=1 & turn=2
    then go to L 
    < critical section>
c2=0;
```

- turn = i ensures that only process i can wait
- variables c1 and c2 ensure mutual exclusion

*Solution for n processes was given by Dijkstra and is quite tricky!*
Analysis of Dekker’s Algorithm

Scenario 1

Process 1
\[ c_1 = 1; \]
\[ \text{turn} = 1; \]
\[ L: \text{if } c_2 = 1 \& \text{turn} = 1 \]
\[ \text{then go to } L \]
\[ < \text{critical section}> \]
\[ c_1 = 0; \]

Process 2
\[ c_2 = 1; \]
\[ \text{turn} = 2; \]
\[ L: \text{if } c_1 = 1 \& \text{turn} = 2 \]
\[ \text{then go to } L \]
\[ < \text{critical section}> \]
\[ c_2 = 0; \]

Scenario 2

Process 1
\[ c_1 = 1; \]
\[ \text{turn} = 1; \]
\[ L: \text{if } c_2 = 1 \& \text{turn} = 1 \]
\[ \text{then go to } L \]
\[ < \text{critical section}> \]
\[ c_1 = 0; \]

Process 2
\[ c_2 = 1; \]
\[ \text{turn} = 2; \]
\[ L: \text{if } c_1 = 1 \& \text{turn} = 2 \]
\[ \text{then go to } L \]
\[ < \text{critical section}> \]
\[ c_2 = 0; \]
N-process Mutual Exclusion

Lamport’s Bakery Algorithm

Process $i$

Entry Code

Initially $\text{num}[j] = 0$, for all $j$

$\text{choosing}[i] = 1$;
$\text{num}[i] = \max(\text{num}[0], \ldots, \text{num}[N-1]) + 1$;
$\text{choosing}[i] = 0$;

for($j = 0; j < N; j++$) {
    while( $\text{choosing}[j]$ );
    while( $\text{num}[j] \&\&$
        $( \text{num}[j] < \text{num}[i] ) \|$
        $( \text{num}[j] == \text{num}[i] \&\& j < i ) ) );
}

$\text{num}[i] = 0$;

Exit Code
A *semaphore* is a non-negative integer, with the following operations:

\[ P(s): \text{if } s > 0, \text{ decrement } s \text{ by } 1, \text{ otherwise wait} \]

\[ V(s): \text{increment } s \text{ by } 1 \text{ and wake up one of the waiting processes} \]

P’s and V’s must be executed atomically, i.e., without

- *interruptions* or
- *interleaved accesses to* \( s \) *by other processors*

*Process i*

\[ \begin{align*}
P(s) & \\
<\text{critical section}> & \\
V(s) & \\
\end{align*} \]

*initial value of* \( s \) *determines the maximum no. of processes in the critical section*
Implementation of Semaphores

Semaphores (mutual exclusion) can be implemented using ordinary Load and Store instructions in the Sequential Consistency memory model. However, protocols for mutual exclusion are difficult to design...

Simpler solution:

*atomic read-modify-write instructions*

Examples: *m is a memory location, R is a register*
Multiple Consumers Example

*using the Test&Set Instruction*

P: \[\text{Test} & \text{Set (mutex)}, R_{\text{temp}} \]
   \[\text{if } (R_{\text{temp}} \neq 0) \text{ goto P} \]

spin:
\[\text{Load } R_{\text{head}}, (\text{head})\]
\[\text{Load } R_{\text{tail}}, (\text{tail})\]
\[\text{if } R_{\text{head}} == R_{\text{tail}} \text{ goto spin}\]
\[\text{Load } R, (R_{\text{head}})\]
\[R_{\text{head}} = R_{\text{head}} + 1\]
\[\text{Store } (\text{head}), R_{\text{head}}\]

V: \[\text{Store } (\text{mutex}), 0\]
process(R)

Other atomic read-modify-write instructions (Swap, Fetch&Add, etc.) can also implement P’s and V’s

What if the process stops or is swapped out while in the critical section?
Nonblocking Synchronization

\[
\text{Compare&Swap}(m), R_t, R_s:
\]
\[
\text{if } (R_t == M[m])
\]
\[
\quad \text{then } M[m] = R_s;
\]
\[
\quad R_s = R_t;
\]
\[
\quad \text{status } \leftarrow \text{success};
\]
\[
\text{else } \text{status } \leftarrow \text{fail};
\]

status is an implicit argument

try:
\[
\text{Load } R_{\text{head}}, (\text{head})
\]
\[
\text{Load } R_{\text{tail}}, (\text{tail})
\]
\[
\text{if } R_{\text{head}} == R_{\text{tail}} \text{ goto spin}
\]
\[
\text{Load } R, (R_{\text{head}})
\]
\[
R_{\text{newhead}} = R_{\text{head}} + 1
\]
\[
\text{Compare&Swap}(\text{head}), R_{\text{head}}, R_{\text{newhead}}
\]
\[
\text{if } (\text{status} == \text{fail}) \text{ goto try}
\]
\[
\text{process}(R)
\]
Load-reserve & Store-conditional

Special register(s) to hold reservation flag and address, and the outcome of store-conditional

Load-reserve \(R, (m):\)
\[
\text{<flag, adr} \leftarrow \text{<1, m>}; \\
R \leftarrow M[m];
\]

Store-conditional \((m), R:\)
\[
\text{if } \text{<flag, adr} == \text{<1, m> } \\
\text{then cancel other procs’ reservation on m; } \\
M[m] \leftarrow R; \\
\text{status} \leftarrow \text{succeed; } \\
\text{else status} \leftarrow \text{fail; }
\]

try:
spin:

Load-reserve \(R_{\text{head}}, (\text{head})\)
Load \(R_{\text{tail}}, (\text{tail})\)
if \(R_{\text{head}} == R_{\text{tail}} \) goto spin
Load \(R, (R_{\text{head}})\)
\(R_{\text{head}} = R_{\text{head}} + 1\)
Store-conditional \((\text{head}), R_{\text{head}}\)
if (status==fail) goto try process(R)
Performance of Locks

Blocking atomic read-modify-write instructions
  e.g., Test&Set, Fetch&Add, Swap
  vs
Non-blocking atomic read-modify-write instructions
  e.g., Compare&Swap,
  Load-reserve/Store-conditional
  vs
Protocols based on ordinary Loads and Stores

Performance depends on several interacting factors:
degree of contention,
caches,
out-of-order execution of Loads and Stores

later ...
An execution is strongly consistent (linearizable) if the method calls can be correctly arranged retaining the mutual order of calls that do not overlap in time, regardless of what thread calls them.
An execution is quiescently consistent if the method calls can be correctly arranged retaining the mutual order of calls separated by quiescence, a period of time where no method is being called in any thread.
Acknowledgements

- These slides contain material developed and copyright by:
  - Arvind (MIT)
  - Krste Asanovic (MIT/UCB)
  - Joel Emer (Intel/MIT)
  - James Hoe (CMU)
  - John Kubiatowicz (UCB)
  - David Patterson (UCB)

- MIT material derived from course 6.823
- UCB material derived from course CS252
- “New microprocessor claims 10x energy improvement”, from extremetech
- “Exploring the diverse world of programming” by Pavel Shved