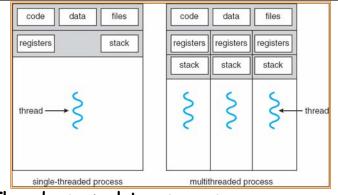
Recall: Modern Process with Multiple Threads

• Process: Operating system abstraction to represent **CS162** what is needed to run a single, multithreaded **Operating Systems and** program Systems Programming • Two parts: - Multiple Threads Lecture 4 » Each thread is a single, sequential stream of execution - Protected Resources: Thread Dispatching » Main Memory State (contents of Address Space) » I/O state (i.e. file descriptors) • Why separate the concept of a thread from that of September 12, 2005 a process? Prof. John Kubiatowicz - Discuss the "thread" part of a process (concurrency) - Separate from the "address space" (Protection) http://inst.eecs.berkeley.edu/~cs162 - Heavyweight Process \equiv Process with one thread 9/12/05 Kubiatowicz CS162 ©UCB Fall 2005 Lec 4.2 **Recall: Single and Multithreaded Processes Recall:** Classification



- · Threads encapsulate concurrency
 - "Active" component of a process
- · Address spaces encapsulate protection
 - Keeps buggy program from trashing the system
 - "Passive" component of a process

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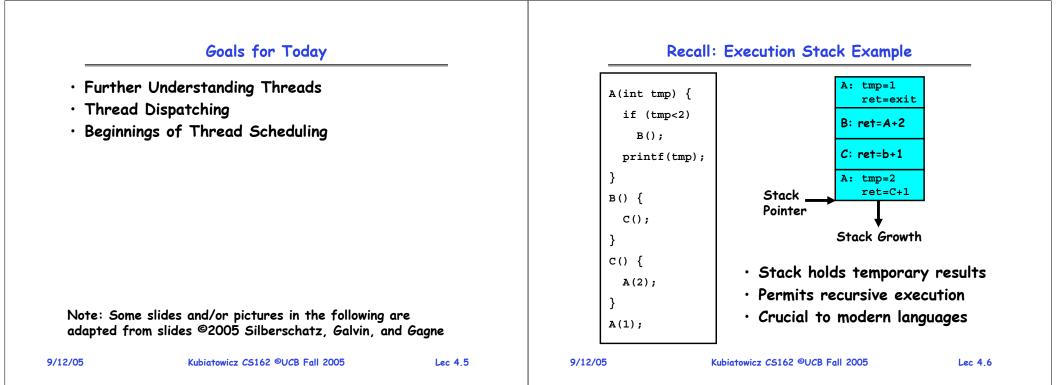
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Lec 4.3

threads to s Per AS: #	One	Many
One	MS/DOS, early Macintosh	Traditional UNIX
Many	Embedded systems (Geoworks, V×Works, JavaOS,etc) JavaOS, Pilot(PC)	Mach, OS/2, Linux Windows 95??? Win NT to XP, Solaris, HP-UX, OS X

Real operating systems have either

- One or many address spaces
- One or many threads per address space
- Did Windows 95/98/ME have real memory protection?
 No: Users could overwrite process tables/System DLLs



MIPS: Software conventions for Registers

0	zer	o constant 0	16 s0 callee saves	
1	at	reserved for assembler	(callee must save)	
2 .	v0	expression evaluation &	23 s7	
3 .	v1	function results	24 t8 temporary (cont'd)	
4	a0	arguments	25 t9	
5 6	a1		26 k0 reserved for OS kernel	
6	a2		27 k1	
7	a3		28 gp Pointer to global area	
8 1	t0	temporary: caller saves	29 sp Stack pointer	
		(callee can clobber)	30 fp frame pointer	
15 1	t7		31 ra Return Address (HW)	

Single-Threaded Example

$\boldsymbol{\cdot}$ Imagine the following C program:

```
main() {
   ComputePI("pi.txt");
   PrintClassList("clist.text");
}
```

- What is the behavior here?
 - Program would never print out class list
 - Why? ComputePI would never finish

- Save ra

- Other things trashed

Lec 4.7

Use of Threads



```
main() {
    CreateThread(ComputePI("pi.txt"));
    CreateThread(PrintClassList("clist.text"));
}
```

- What does "CreateThread" do?
 - Start independent thread running given procedure
- What is the behavior here?

CPU2

Time -

CPU1

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- Now, you would actually see the class list

CPU1

- This should behave as if there are two separate CPUs

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CPU2 CPU1

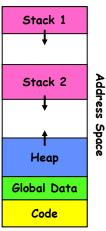
CPU2

• If we stopped this program and examined it with a debugger, we would see - Two sets of CPU registers - Two sets of Stacks

• Questions:

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- How do we position stacks relative to each other?
- What maximum size should we choose for the stacks?
- What happens if threads violate this?
- How might you catch violations?



```
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```

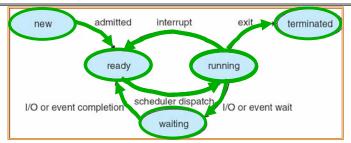
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Per Thread State

- Each Thread has a *Thread Control Block* (TCB)
 - Execution State: CPU registers, program counter, pointer to stack
 - Scheduling info: State (more later), priority, CPU time
 - Accounting Info
 - Various Pointers (for implementing scheduling queues)
 - Pointer to enclosing process? (PCB)?
 - Etc (add stuff as you find a need)
- $\boldsymbol{\cdot}$ In Nachos: "Thread" is a class that includes the TCB
- OS Keeps track of TCBs in protected memory - In Array, or Linked List, or ...

Lifecycle of a Thread (or Process)

Memory Footprint of Two-Thread Example



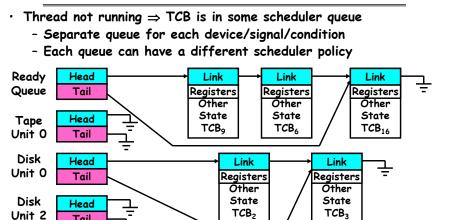
- As a thread executes, it changes state:
 - new: The thread is being created
 - ready: The thread is waiting to run
 - running: Instructions are being executed
 - waiting: Thread waiting for some event to occur
 - terminated: The thread has finished execution
- \cdot "Active" threads are represented by their TCBs

- TCBs organized into queues based on their state 9/12/05 Kubiatowicz C5162 @UCB Fall 2005

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Lec 4.9

Ready Queue And Various I/O Device Queues



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Asside: Implementation Java OS

- Many threads, one Address Space
- Why another OS?

Tail

Head

Tail

Ether

Netwk 0

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- Recommended Minimum memory sizes:

Link

Registers

Other

State

TCB₈

- » UNIX + X Windows: 32MB
- » Windows 98: 16-32MB
- » Windows NT: 32-64MB

» Windows 2000/XP: 64-128MB

- What if want a cheap network point-of-sale computer?
 - » Say need 1000 terminals
 - » Want < 8MB
- What language to write this OS in?
 - C/C++/ASM? Not terribly high-level. Hard to debug.
- Java/Lisp? Not guite sufficient need direct access to HW/memory management Kubiatowicz CS162 ©UCB Fall 2005 9/12/05

Java OS Structure Java APPS 05 Hardware

Lec 4,15

Lec 4.13

Administrivia

- · Group assignments now posted on website - Check out the "Group/Section Assignment" link
 - Please attend your newly assigned section
- Nachos readers:
 - Available from Northside Copy Central
 - Includes printouts of all of the code
- Warning: you will be prompted for a passphrase
 - We need to autogenerate ssh keys for you
 - When prompted for a pass phrase, don't forget it!
 - This is needed for group collaboration tools
- Not everyone has run the register program!
 - This should happen automatically when you login, but you need to avoid hitting control-C
- Time to start Project 1
 - Go to Nachos page and start reading up
- Start reading through the Nachos code (reader) 9/12/05 Lec 4.14

Dispatch Loop

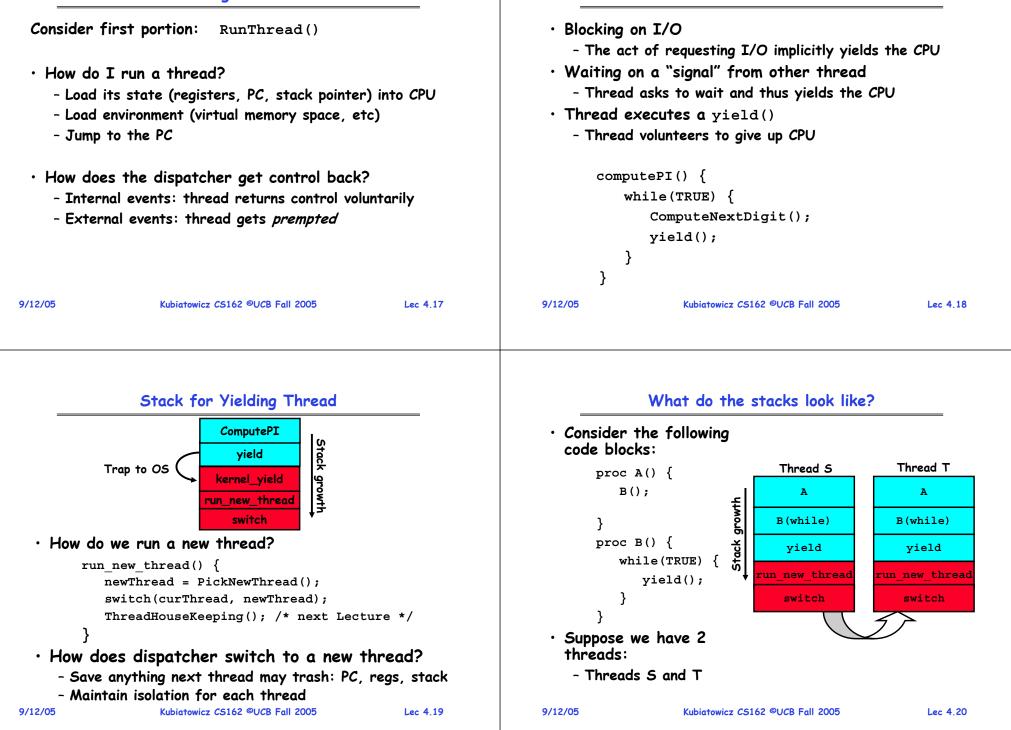
- · Conceptually, the dispatching loop of the operating system looks as follows:
 - Loop { RunThread(): ChooseNextThread(); SaveStateOfCPU(curTCB); LoadStateOfCPU(newTCB);
- This is an *infinite* loop

}

- One could argue that this is all that the OS does
- Should we ever exit this loop???
 - When would that be?
 - Emergency crash of operating system called "panic()"



Internal Events



aving/Restoring state (often called "Contex Switch(tCur,tNew) {	 How many registers need to be saved/restored? 			
/* Unload old thread */		- MIPS 4k: 32 Int(32b), 32 Float(32b) - Pentium: 14 Int(32b), 8 Float(80b), 8 SSE(128b),		
TCB[tCur].regs.r7 = CPU.r7;				
TCB[tCur].regs.r0 = CPU.r0;		 Sparc(v7): 8 Regs(32b), 16 Int regs (32b) * 8 windows = 136 (32b)+32 Float (32b) Itanium: 128 Int (64b), 128 Float (82b), 190ther(64b retpc is where the return should jump to. In reality, this is implemented as a jump There is a real implementation of switch in Nachos. 		
TCB[tCur].regs.sp = CPU.sp; TCB[tCur].regs.retpc = CPU.retpc; /*ret	urn addr*/			
<pre>/* Load and execute new thread */</pre>				
CPU.r7 = TCB[tNew].regs.r7;				
 CPU.r0 = TCB[tNew].regs.r0; CPU.sp = TCB[tNew].regs.sp;			ally, switch is implemented as assembly!	
CPU.retpc = TCB[tNew].regs.retpc; return; /* Return to CPU.retpc */		- Of course, it's magical! - But you should be able to follow it!		

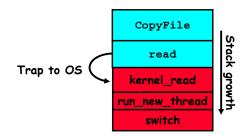
Switch Details (continued)

- What if you make a mistake in implementing switch?
 - Suppose you forget to save/restore reg 4
 - Get intermittent failures depending on when context switch occurred and whether new thread uses reg 4
 - System will give wrong result without warning
- \cdot Can you devise an exhaustive test to test switch code?
 - No! Too many combinations and inter-leavings
- Cautionary tail:
 - For speed, Topaz kernel saved one instruction in switch()
 - Carefully documented!
 - What happened?
 - » Time passed, People forgot
 - » Later, they added features to kernel (noone removes features!)
 - » Very weird behavior started happening
 - Moral of story: Design for simplicity

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05 Lec 4.23

What happens when thread blocks on I/O?



• What happens when a thread requests a block of data from the file system?

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- User code invokes a system call
- Read operation is initiated
- Run new thread/switch
- Thread communication similar
 - Wait for Signal/Join
 - Networking

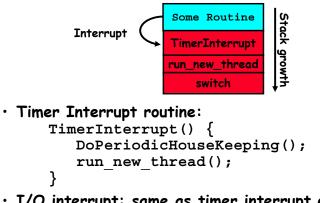
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External Events

Example: Network Interrupt Raise priority • What happens if thread never does any $I/O_{.}$ eenable All Ints? never waits, and never yields control? Save registers Jo Interrupt add \$r1,\$r2,\$r3 - Could the ComputePI program grab all resources Dispatch to Handle subi \$r4,\$r1,#4 2 and never release the processor? slli \$r4,\$r4,#2 and Transfer Network » What if it didn't print to console? Packet from hardware Pipeline Flush - Must find way that dispatcher can regain control! External to Kernel Buffers Interrupt Answer: Utilize External Events \$r2,0(\$r4) ٦ω 1w \$r3.4(\$r4) - Interrupts: signals from hardware or software Restore registers \$r2,\$r2,\$r3 add that stop the running code and jump to kernel Clear current Int 8(\$r4),\$r2 CT 147 Disable All Ints - Timer: like an alarm clock that goes off every Restore priority some many milliseconds RTI • If we make sure that external events occur • An interrupt is a hardware-invoked context switch frequently enough, can ensure dispatcher runs - No separate step to choose what to run next - Always run the interrupt handler immediately Kubiatowicz CS162 ©UCB Fall 2005 9/12/05 Kubiatowicz CS162 ©UCB Fall 2005 Lec 4.25 9/12/05 Lec 4.26

Use of Timer Interrupt to Return Control

• Solution to our dispatcher problem - Use the timer interrupt to force scheduling decisions



• I/O interrupt: same as timer interrupt except that DoHousekeeping() replaced by ServiceIO().

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Choosing a Thread to Run

- How does Dispatcher decide what to run?
 - Zero ready threads dispatcher loops
 - » Alternative is to create an "idle thread"
 - » Can put machine into low-power mode
 - Exactly one ready thread easy
 - More than one ready thread: use scheduling priorities
- Possible priorities:
 - LIFO (last in, first out):
 - » put ready threads on front of list, remove from front
 - Pick one at random
 - FIFO (first in, first out):
 - » Put ready threads on back of list, pull them from front
 - » This is fair and is what Nachos does
 - Priority gueue:
- » keep ready list sorted by TCB priority field 9/12/05

Summary

- \cdot The state of a thread is contained in the TCB
 - Registers, PC, stack pointer
 - States: New, Ready, Running, Waiting, or Terminated
- Multithreading provides simple illusion of multiple CPUs
 - Switch registers and stack to dispatch new thread
 - Provide mechanism to ensure dispatcher regains control
- \cdot Switch routine
 - Can be very expensive if many registers
 - Must be very carefully constructed!
- Many scheduling options
 - Decision of which thread to run complex enough for complete lecture

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