

Atomic Read-Modify-Write instructions

· Problems with interrupt-based lock solution: - Can't give lock implementation to users - Doesn't work well on multiprocessor » Disabling interrupts on all processors requires messages and would be very time consuming Alternative: atomic instruction sequences - These instructions read a value from memory and write a new value atomically - Hardware is responsible for implementing this correctly » on both uniprocessors (not too hard) » and multiprocessors (requires help from cache coherence protocol) - Unlike disabling interrupts, can be used on both uniprocessors and multiprocessors 2/6/13 Lec 5.3 Ion Stoica and Anthony D. Joseph CS162 ©UCB Spring 2013



Lec 5.2













	Where are we going with synchronization?	
Programs	Shared Programs	
Higher- level API	Locks Semaphores Monitors Send/Receive	
Hardware	Load/Store Disable Ints Test&Set Comp&Swap	
 We are g synchror Every and st Need 	going to implement various higher-level nization primitives using atomic operations hing is pretty painful if only atomic primitives are load ore to provide primitives useful at user-level	











Discussion about Solution			
 Is order of P's important? Is order of V's important? No, except that it might affect scheduling efficiency What if we have 2 producers or 2 consumers? 	<pre>Producer(item) { mutex.P(); emptySlots.P(); Enqueue(item); mutex.V(); fullSlots.V(); } Consumer() { fullSlots.P(); mutex.P(); item = Dequeue(); mutex.V(); emptySlots.V(); return item; }</pre>		
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