CS250 VLSI Systems Design

L6: Class Project Ideas

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General Project Info

- Most significant component of class (70% of grade!)
- Intent is to give you all a large-scale VLSI design experience in a team setting
- Work in teams of 2 or 3 (preferred)
Project Topics

- Four predefined topic areas related to the ParLab “InfiniCore” manycore processor design:
  - Processor + vector-thread core
  - Processor private memory interface
  - Processor-memory interconnect
  - DRAM access scheduler and controller
  - ...more later

- Or, your own project idea
  - But we’ll need some convincing you know what you’re doing
Our Project Expectations

- B grade
  - Single working design

- A grade
  - Thorough design-space exploration
Results from MIT Lab Exercise (6.884 2005)

Lab 2 ASIC Implementation Results

Pareto-Optimal Points
Metrics: Area, Energy, Performance

- Area in mm\(^2\)
- Energy in Joules/Operation
- Performance in Operations/Second

- Ideally, generate Pareto-Optimal points in these three dimensions
Project Meetings/Timeline

- Class splits into two sets of project groups. One half meets on Tuesday, one on Thursday.
- Each meeting has a milestone due, and is designed so we can give feedback.
- Four project group meetings:
  - Oct 8: Initial project proposal due
  - Oct 13/15: Review initial project proposal
  - Oct 27/29: Review functional model/test harness
  - Nov 10/12: Review initial arch/uarch design
  - Dec 1/3: Review design space exploration results
- Plus, come to office hours, arrange other meetings
Initial Proposal

- Due October 8
- Title
- Team members
- 2-page PDF description of what you want to do
- Where you will get functional model, test infrastructure.
- Initial guess at high-level block diagram.
- What does the design space look like and how you will explore it.
Functional Model/Test Harness

- Have to build functional model (C/C++?) and test harness first.
- Test harness also includes architectural level test suite (Black-box testing)

- Due in project meetings on Oct 27/29
- Want to see your functional model passing your test suite, and evidence you have good coverage of functionality
Initial Arch/μArch Design

- Need to complete a single working RTL design that represents one point in design space
- Need white-box test suite that verifies operation of μarch (e.g., bypasses)

- Due in project meetings Nov 10/12
- We want to see one complete RTL design passing your “white-box” test suite
Design-Space Exploration

› Need several, hopefully many, instances of your design with Pareto-Optimal points
› All of these should pass tests
› Due in project meetings Dec 1-2
Final Presentation/Report

- 20 minute presentation to whole class on Dec 8 (whole day schedule, time/location TBD)
- Final project report
  - like a conference paper, <=12 pages, two-column, PDF
- Report due 9AM Monday Dec 14
  - No extensions!