Outline

Standard cell “back-end” place and route tools make layout mostly automatic. However, you should understand some of the more difficult concerns for physical implementation:

- Power distribution
- Chip input/output
- Clock distribution
- Floor-planning

- Not: Place & Route
Routing PWR and GND

Main Design Concerns:

1. IR Drops. Remembering Ohms Law $V = IR$.
   Voltage drops due to resistance in power/GND wires ⇒ slower circuits, false switching

2. Metal Migration (electromigration).
   Accidental fusing ⇒ chip failure

3. Inductive Effects.
   Bounce and oscillation on power nodes ⇒ false switching

Metal Migration

- A current flux through a metal conductor exceeding a certain limit causes metal atoms to move in the direction of the current.

- If there is a small constriction ...
  - the current density will be higher and more metal atoms will be carried away, creating a higher current density, ..., ⇒ open circuit

- Metal migration begins at $\sim 2 \times 10^5$ A/cm²

- Design Guideline: Size width of both Vdd and GND wires so that no more than $\sim 0.5$ mA/um in width (aluminum).
Other Migration Related Failures

**FIGURE 2.35** Electromigration-related failure modes. (a) A broken line caused by removal of metal molecules with electromigration. (b) An undesired short circuit caused by a whisker-like structure formed by accumulation of metal molecules transported by electromigration. These “whiskers” are observed to grow as long as 100 “m. (c) A “hillock” that goes through the insulator between the two adjoining interconnection levels causing a short circuit.

IR Drops

1. Slower circuit operation because of series resistance with transistors:

   \[ Z = (R_w + R_p) C_L \]
IR Drops

- Switching induced noise on pwr and GND rails can couple through to logic signals and cause accidental switching.
- Particularly troublesome around circuit with low noise immunity. Ex: RAM block sense amplifiers.

Layout Strategy for Power Rails (power and ground wires)

1. Keep distance from source of power as short as possible.
2. Use wide/thick metal.
3. Isolate "noisy" sections.
4. Use multiple sources.
Layout Strategy for Power Rails (power and ground wires)

- With many layers of metal, upper few layers are typically thicker than lower layers.
- Upper layers get allocated for global power rails.
- Via connections to lower layers for local distribution.

Inductive Bounce

Inductance in the power and ground paths results in voltage glitches (noise) on Vdd and GND nodes.

On-chip L values of wires is small => usually not significant except:
1. Very large currents: clock drivers, off-chip drivers
2. Package pins, bonding wires (1nH/mm)
   - Package pins can have from 2-40nH of inductance, depending on package type

Strategy:
1. Use multiple bonding pads (wires) from Vdd & GND
2. If necessary, use on-chip bypass capacitors
On-chip Bypass Capacitors

- When transistors switch, current is drawn from $C_D$ rather than through package pins and bonding wires - smoothes out $\frac{dl}{dt}$. (Think of it as a "charge cache").

- Gate oxide leads to highest capacitance, but poor yield. Thicker oxides are used.

On-chip Bypass Capacitance

- Distributed bypass capacitors also smooth out noise from IR drops by locally supplying charge when needed.

- Generally, capacitance on Vdd and GND is a good thing. (Fat wires help, larger transistor source regions help, extra capacitors when needed)

- Capacitive bypassing continues all the way up the packaging chain.
Bypass Capacitors

- On-chip bypass capacitors are not effective for off-chip drivers:

  - On-chip capacitors keep the voltage difference across the power lines stable but cannot prevent the on-chip power-supply levels from moving up and down w.r.t. the board power-supply levels.
  - Therefore, high-speed chip outputs are surrounded by many pwr and ground connections (pins). Example GTPs on Xilinx FPGAs, Memory interface on processors and bridge chips.

Package Connections

- "Pads": Special cells in the "design kit" for the layout generator.
  - Pad (metal layer build-up), for wire bonding or solder-ball
  - Circuitry provides ESD protection, drive strength for output, input buffering, registering of signals, etc.
  - Classic example of large capacitive fan-out. Internal capacitances on order of femto-farads, external ones are pico-farads. Uses staged drivers.
Electro-static Discharge (ESD) and Over-voltage Protection

FIGURE 5.56 An electrostatic model of a person. (a) Physical configuration; (b) Equivalent circuit.

FIGURE 2.30 Improved CMOS input protection circuitry. Sturdy but less sensitive protection devices are placed at the front to filter out gross voltage and current spikes. Later more sensitive devices clamp the smaller spikes that pass through the first stage.

I/O Floorplan

“Perimeter” pads is the classic arrangement.

- Signals get routed from chip core to periphery.
- Perimeter $\propto \sqrt{\text{area}}$
- At 200um pitch $\Rightarrow$ 100 pads max per side (2cm die)
- Most commonly used for wire bond attachment.

"Perimeter" pads is the classic arrangement.
**I/O Floorplan**

Area pads allow higher number of connections.

- Allow up to thousands of connections.
- Wire-bonding no longer possible => "flip-chip" technologies.

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**Flip-chip Bonding**

- In addition to higher density, lower resistance and inductance.
- Eases layout of circuits and power/clk distribution (signals come-in/go-out closer to where needed).
Clock Distribution

A challenging consequence of the synchronize design methodology is a need to distribute a clock signal in synchrony to every state element - and do so with low-power (this challenge has driven some to asynchronous circuit design).

Clock skew can create both setup and hold problems.

Clock Skew Related Failure

- If clock period $T = T_{CL} + T_{setup} + T_{clk} - Q + T_{skew}$, circuit will fail with setup time violation.
- This problem can be fixed by increasing the clock period.

- If $T_{CL} < T_{skew}$, circuit will fail with hold time violation.
- Increasing the clock period will not help. Need to add delay.
"Leaf" wires end up being long and therefore small variations in length create large variation in delay (L² effect).

One approach is to use wide wires to minimize R.

Use successfully in Alpha microprocessors (and others). But high power consumption.

RC delay of each path must be controlled.
Load must be balanced.

Load must be balanced.
Match strength all drivers within a level.

Now standard practice.
Clock Tree Layout

Standard synthesis tools take "clock uncertainty into account". Layout tools will automatically layout a low-skew clock tree. Advanced tools analyze and take into account clock skew between pairs of state-elements.

Clock Distribution Examples

Xilinx Virtex FPGA
Clock Tree Delays, IBM “Power” CPU

Clock Tree Delays, IBM Power
PLLs or DLLs often build on-chip to deskew chip core relative to PCB environment. They also get used for clock frequency multiplication.

Floorplanning Strategies

Pay attention to communication - data- and control-flow

- Wiring can account for the majority of the power consumption and area.
- Automatic layout tools do this locally. Global floorplanning (placement of large blocks) may need to be specified.
Floorplanning Strategies

Exploit Regularity

- Simplifies layout and verification. Create sub-block and instantiate many times.
- Helps in manufacturability and yield enhancement.
- Examples: FPGAs, memory blocks, bit-slice processor datapaths, systolic arrays, ...

Next Time

- Chip layout examples ...