Simulating Verilog RTL using Synopsys VCS

CS250 Tutorial 4 (Version 091209a)
September 12, 2010
Yunsup Lee

In this tutorial you will gain experience using Synopsys VCS to compile cycle-accurate executable simulators from Verilog RTL. You will also learn how to use the Synopsys Waveform viewer to trace the various signals in your design. Figure 1 illustrates the basic VCS toolflow and RISC-V toolchain. For more information about the RISC-V toolchain consult *Tutorial 3: Build, Run, and Write RISC-V Programs*.

VCS takes a set of Verilog files as input and produces a simulator. When you execute the simulator you need some way to observe your design so that you can measure its performance and verify that it is working correctly. There are two primary ways to observe your design: (1) you can use `$display` statements in your Verilog RTL to output textual trace information, or (2) you can instruct the simulator to automatically write transition information about each signal in your design to a file. There is standard text format for this type of signal transition trace information called the Value Change Dump format (VCD). Unfortunately, these textual trace files can become very large very quickly, so Synopsys uses a proprietary compressed binary trace format called VCD Plus (VPD). You can view VPD files using the Synopsys waveform viewer called Discovery Visual Environment (DVE).

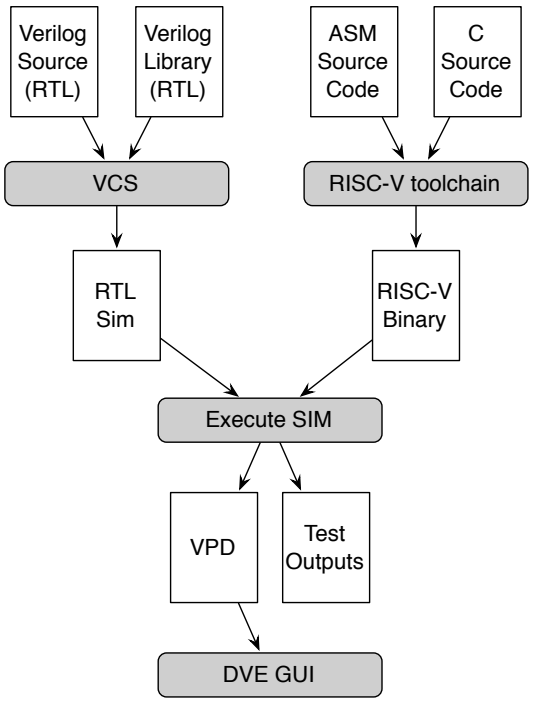

Figure 1: VCS Toolflow and RISC-V Assembler Toolchain

You will be using a simple unpipelined RISC-V v1 processor as your design example for this tutorial, and thus you will also learn how to build and run test codes on the processor simulator. Figure 2 shows the block diagram for the example processor. Figure 1 shows the RISC-V toolchain which starts with an RISC-V assembly file and generates a binary file suitable to run on the cycle-accurate simulator. This tutorial assumes you are familiar with the RISC-V ISA. For more information please consult the *RISC-V Processor Specification*.

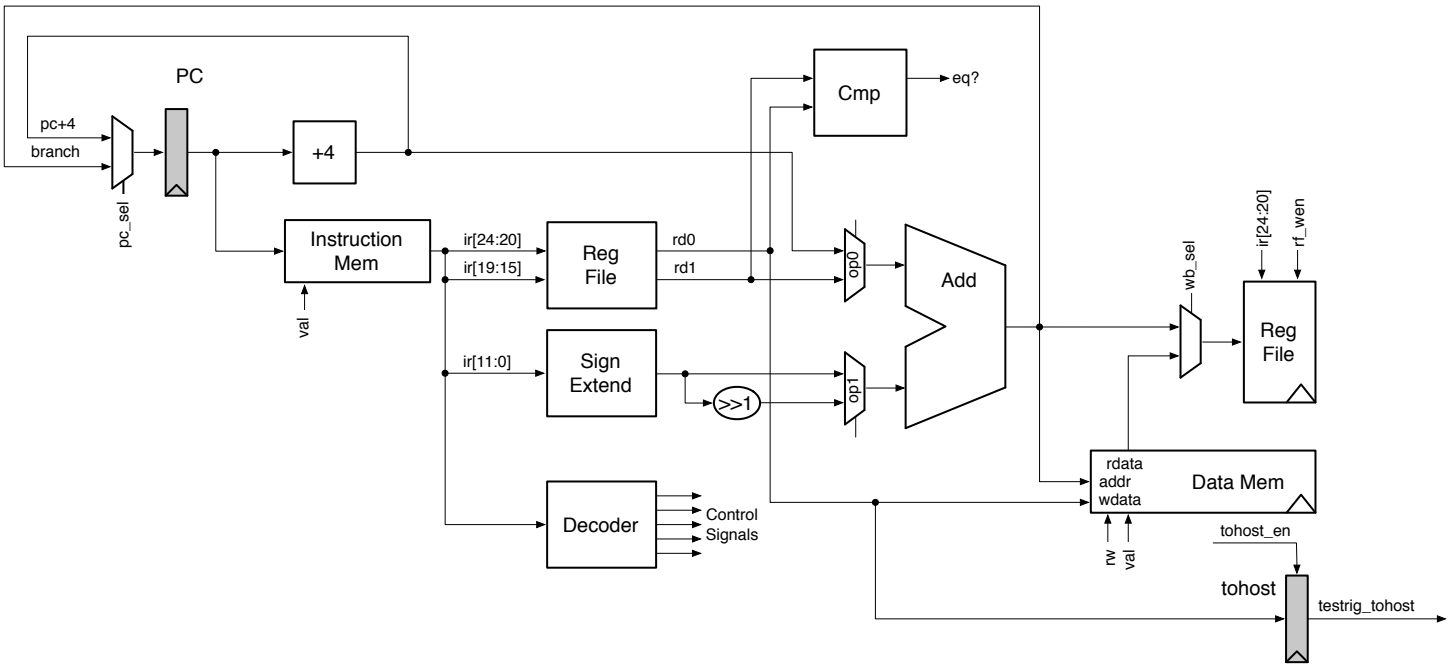

Figure 2: Block diagram for Unpipelined RISC-V v1 Processor

The following documentation is located in the course locker `~cs250/manuals` and provides additional information about VCS, DVE, and Verilog.

- `vcs-user-guide.pdf` - VCS User Guide
- `vcs-quick-reference.pdf` - VCS Quick Reference
- `vcs_dve-user-guide.pdf` - Discovery Visual Environment User Guide
- `vcs_ucli-user-guide.pdf` - Unified Command Line Interface User Guide
- `ieee-std-1364-1995-verilog.pdf` - Language specification for the original Verilog-1995
- `ieee-std-1364-2001-verilog.pdf` - Language specification for Verilog-2001
- `ieee-std-1364-2005-verilog.pdf` - Language specification for Verilog-2005
- `ieee-std-1364.1-2002-verilog-synthesis.pdf` - Standard for Verilog Register Transfer Level Synthesis
- `ieee-std-1800-2005-sysverilog.pdf` - Language specification for the original SystemVerilog-2005
- `ieee-std-1800-2009-sysverilog.pdf` - Language specification for SystemVerilog-2009

Getting started

You can follow along through the tutorial yourself by typing in the commands marked with a '%' symbol at the shell prompt. To cut and paste commands from this tutorial into your bash shell (and make sure bash ignores the '%' character) just use an alias to "undefine" the '%' character like this:

```
% alias %=""
```

All of the CS250 tutorials should be ran on an EECS Instructional machine. Please see the course website for more information on the computing resources available for CS250 students. Once you have logged into an EECS Instructional you will need to setup the CS250 toolflow with the following commands.

```
% source ~cs250/tools/cs250.bashrc
```

For this tutorial you will be using an unpipelined RISC-V v1 processor as your example RTL design. Create a working directory and copy files from the course locker using the following commands.

```
% mkdir tut4
% cd tut4
% TUTROOT=$PWD
% cp -R ~cs250/examples/v-riscv-v1-1stage/* $TUTROOT
```

Before starting, take a look at the subdirectories in the project directory. All of your projects will have a similar structure. Source RTL should be placed in the `src` directory and test input files should be placed in the `riscv-tests` directory. The `build` directory will contain all generated content including simulators, synthesized gate-level Verilog, and final layout. In this course you will always try to keep generated content separate from your source RTL. This keeps your project directories well organized, and helps prevent you from unintentionally modifying your source RTL. There are subdirectories in the `build` directory for each major step in the CS250 toolflow. These subdirectories will contain scripts and configuration files necessary for running the tools required for that step in the toolflow. For example, the `build/vcs-sim-rtl` directory contains a makefile which can build Verilog simulators and run tests on these simulators. For more information, please consult *Tutorial 2: Bits and Pieces of CS250's toolflow*. You should browse the source code for the processor in `src` to become familiar with the design. The `csrc` directory contains Direct C source files. These C source files are used in the Verilog test harness to simulate memory, parse and load ELF files. Direct C is a very convenient way to glue Verilog simulation with C functions, which will be used through out the course. Please refer to the VCS user guide chapter 19 (C Language Interface) for more information on Direct C.

Compiling the Simulator

In this section you will first see how to run VCS from the command line, and then you will see how to automate the process using a makefile. To build the simulator you need to run the `vcs` compiler with the appropriate command line arguments and a list of input Verilog files.

```
% cd $TUTROOT/build/vcs-sim-rtl
% vcs -full64 -PP +lint=all,noVCDE +v2k -timescale=1ns/10ps \
      +vc+list -CC "-I$VCS_HOME/include" \
      +define+CLOCK_PERIOD=1.25 \
      +define+IMEM_DELAY=0.4 \
      +define+DMEM_DELAY=0.4 \
      ../../src/defCommon.vh \
      ../../src/riscvInst.vh \
      ../../src/riscvConst.vh \
      ../../src/riscvProcCtrl.v \
      ../../src/riscvProcDpathRegfile.v \
      ../../src/riscvProcDpath.v \
      ../../src/riscvProc.v \
      ../../src/riscvTestHarness.v \
      ../../csrc/elf.cc \
      ../../csrc/memif.cc \
      ../../csrc/main.cc \
```

By default, VCS generates a simulator named `simv`. The `-full64` command line argument makes you use the 64-bit version. `-PP` command line argument turns on support for using the `VPD` trace output format. The `+lint=all,noVCDE` argument turns on Verilog warnings except the VCDE warning. Since it is relatively easy to write legal Verilog code which is probably functionally incorrect, you will always want to use this argument. For example, VCS will warn you if you connect nets with different bitwidths or forget to wire up a port. Always try to eliminate all VCS compilation errors *and* warnings. Since you will be making use of various Verilog-2001 language features, you need to set the `+v2k` command line option so that VCS will correctly handle these new constructs. Verilog allows a designer to specify how the abstract delay units in their design map into real time units using the `‘timescale` compiler directive. To make it easy to change this parameter you will specify it on the command line instead of in the Verilog source. `+vc+list -CC "-I$VCS_HOME/include"` arguments let you compile Direct C. After these arguments you list the Verilog source files and Direct C source files. After running this command, you should see text output indicating that VCS is parsing the Verilog files and compiling the modules. Notice that VCS actually generates ANSI C code which is then compiled using `gcc`. When VCS is finished you should see a `simv` executable in the build directory.

Typing in all the Verilog source files on the command line can be very tedious, so you will use makefiles to help automate the process of building your simulators. The following commands will first delete the simulator you previously built, and then regenerate it using the makefile.

```
% cd $TUTROOT/build/vcs-sim-rtl
% rm -f simv
% make
```

The make program uses the `Makefile` located in the current working directory to generate the file given on the command line. Take a look at the `Makefile` located in `build/vcs-sim-rtl`. Makefiles are made up of variable assignments and a list of rules in the following form.

```
target : dependency1 dependency2 ... dependencyN
    command1
    command2
    ...
    commandN
```

Each rule has three parts: a target, a list of dependencies, and a list of commands. When a desired target file is "out of date" or does not exist, then the make program will run the list of commands to generate the target file. To determine if a file is "out of date", the make program compares the modification times of the target file to the modification times of the files in the dependency list. If any dependency is newer than the target file, make will regenerate the target file. Locate in the makefile where the Verilog source files are defined. Find the rule which builds `simv`. More information about makefiles is online at `http://www.gnu.org/software/make/manual`.

Not all make targets need to be actual files. For example, the `clean` target will remove all generated content from the current working directory. So the following commands will first delete the generated simulator and then rebuild it.

```
% cd $TUTROOT/build/vcs-sim-rtl
% make clean
% make simv
```

Building RISC-V Test Assembly Programs

A test program called `riscv-v1_example.S` is located locally in the `riscv-tests` directory. If you want to add your own test programs, you would add them to this directory. There are additional globally installed RISC-V assembly test programs located in `~cs250/install/riscv-tests` which you can use for your lab assignments and projects. The following command will build all of the local tests and run it on the RISC-V v2 ISA simulator.

```
% cd $TUTROOT/riscv-tests
% make
% make run
```

Please refer to *Tutorial 3: Build, Run, and Write RISC-V Programs* for more information about building, running, and writing assembly test programs.

Running the Simulator and Viewing Trace Output

Now that you have learned how to build the simulator and how to build RISC-V test assembly programs, you will learn how to execute RISC-V test assembly programs on the simulator. The following command runs the local `riscv-v1_example.S` test program on the simulator.

```
% cd $TUTROOT/build/vcs-sim-rtl
% ./simv +exe=$TUTROOT/riscv-tests/riscv-v1_example
```

Try running a globally installed RISC-V test assembly program.

```
% cd $TUTROOT/build/vcs-sim-rtl
% ./simv +exe=$UCB_VLSI_HOME/install/riscv-tests/riscv-v1_addiw
```

You should see some textual trace output showing the state of the processor on each cycle. The trace output includes the cycle number, reset signal, pc, instruction bits, register file accesses, testrig_tohost signal, and the disassembled instruction. The test program does a series of loads and verifies that the loaded data is correct. After running all the tests, the program writes a one into the `tohost` coprocessor register to indicate that all tests have passed. If any test fails, the program will write a number greater than one into the `tohost` register. The test harness waits until the `testrig_tohost` signal is non-zero and displays either `PASSED` or `FAILED` as appropriate.

In addition to the textual output, you should see a `vcdplus.vpd` in your build directory. Use the following command to start the Synopsys Discovery Visual Environment (DVE) waveform viewer and open the generated VPD file.

```
% dve -vpd vcdplus.vpd &
```

Figure 3 shows the DVE Hierarchy window. You can use this window to browse the design's module hierarchy. Choose *Window* > *New* > *Wave View* to open a waveform viewer (see Figure 4). To add signals to the waveform window you can select them in the Hierarchy window and then right click to choose *Add to Waves* > *Recent*.

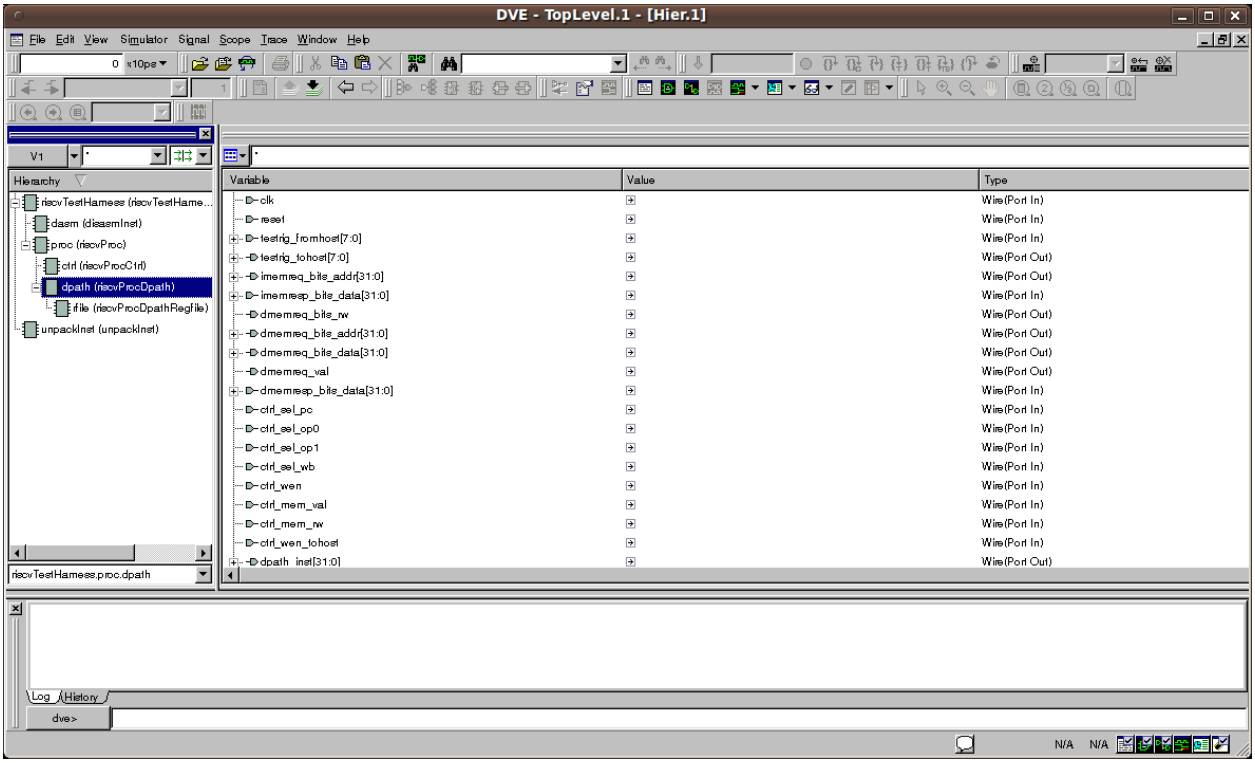

Figure 3: DVE Module Hierarchy Window

Add the following signals to the waveform viewer.

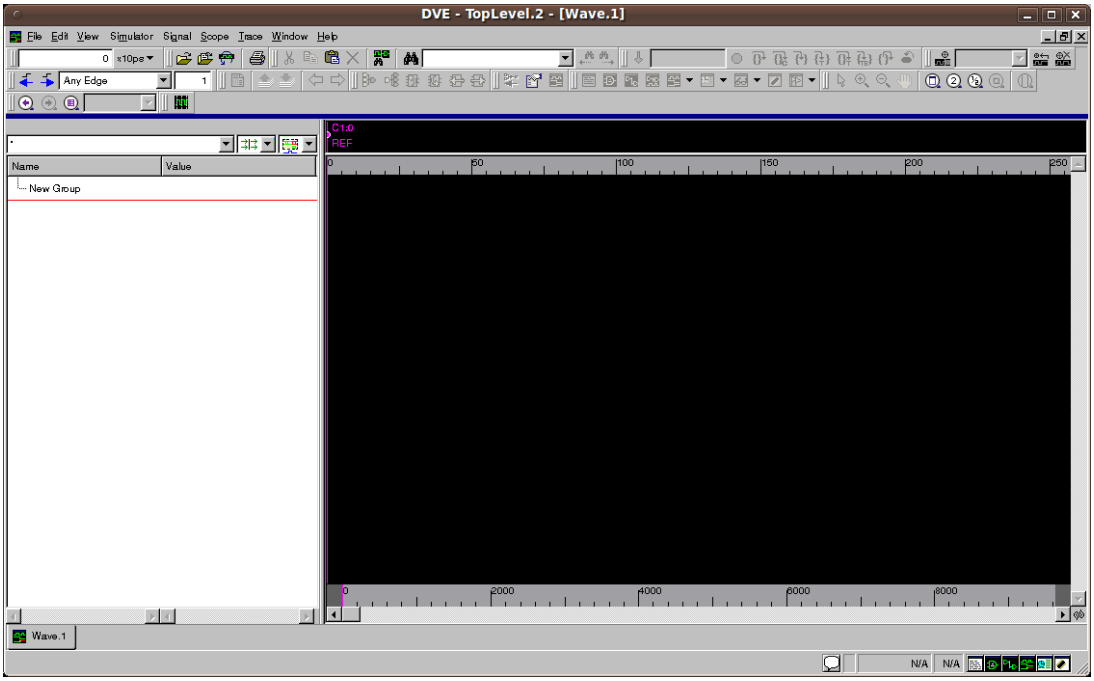

Figure 4: DVE Waveform Window

- `riscvTestHarness.clk`
- `riscvTestHarness.proc.dpath.ctrl_sel_pc`
- `riscvTestHarness.proc.dpath.pc_reg`
- `riscvTestHarness.proc.dpath.raddra`
- `riscvTestHarness.proc.dpath.rdataa`
- `riscvTestHarness.proc.dpath.raddrb`
- `riscvTestHarness.proc.dpath.rdatab`
- `riscvTestHarness.proc.dpath.ctrl_wen`
- `riscvTestHarness.proc.dpath.waddr`
- `riscvTestHarness.proc.dpath.wdata`
- `riscvTestHarness.dasm.minidasm`
- `riscvTestHarness.testrig_tohost`

The `dasm` module is a special tracing module which includes Verilog behavioral code to disassemble instructions. The `minidasm` signal is a short text string which is useful for identifying which instruction is executing during each cycle. To display this signal as a string instead of a hex number, right click on the signal in the waveform viewer. Choose *Set Radix* > *ASCII* from the popup menu. You should now see the instruction type in the waveform window. Use *Zoom* > *Zoom Out* to zoom out so you can see more of the trace at once. Figure 5 shows the waveforms in more detail. You should be able to identify the `addiw` instructions correctly loading the register file with various constants and the `addiw` instructions writing the correct result into the register file. The `ctrl_sel_pc` control signal should remain low until the very end of the program when the code branches to the pass code where it sets the `tohost` register to one.

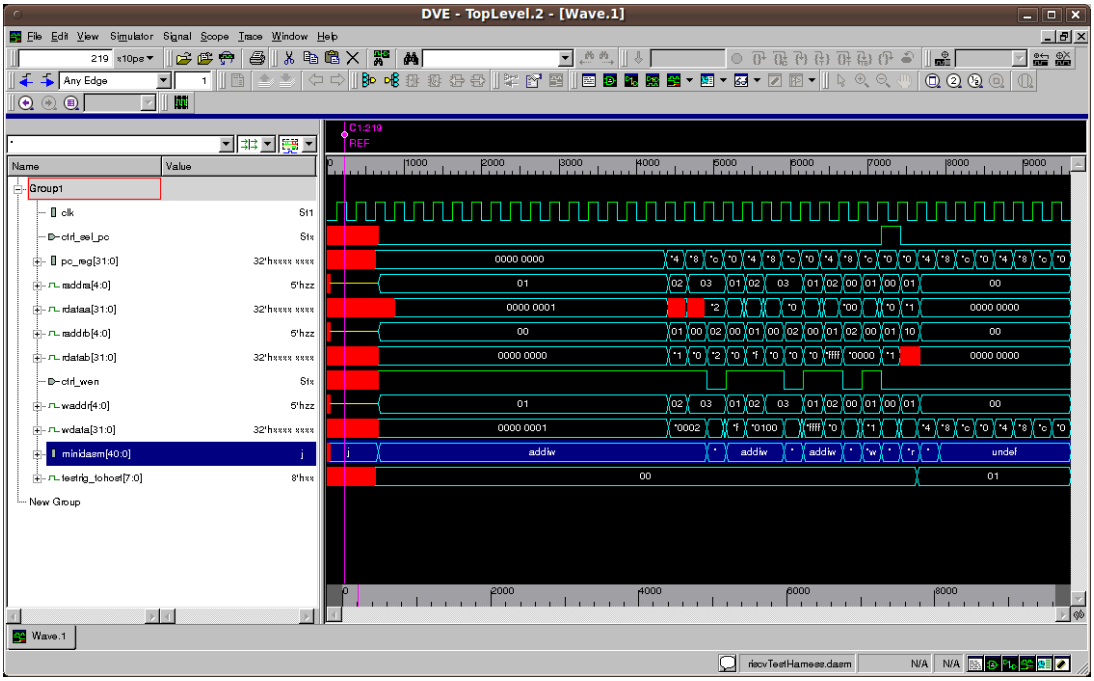

Figure 5: Waveforms for unpipelined RISC-V v1 processor executing `riscv-v1_addiw`

The Verilog test harness provides two optional command line arguments in addition to the required `+exe` argument as shown below:

```
simv +exe=<vmh-filename>
     +max-cycles=<integer>
     +verbose=<0|1>
```

By default, the harness will run for 2,000 cycles. This limit helps prevent bugs in test programs or the RTL from causing the simulator to run forever. When there is a timeout, the harness will display `*** FAILED *** timeout`. The `+max-cycles` argument allows you to increase this limit and is required for longer running programs. If the `+verify` argument is set to one (the default), then the harness will execute in "verification mode". This means that the harness waits until `testrig_tohost` is non-zero and then outputs either `PASSED` or `FAILED` as appropriate. If the `+verify` argument is set to zero, then the harness will execute in "performance mode". This means that the harness waits until `testrig_tohost` is non-zero and then it outputs a collection of statistics. You should use "verification mode" for running test programs which verify the correctness of your processor, and you should use "performance mode" for running benchmarks to evaluate the performance of your processor. Try running the the `riscv-v1_addiw` program in "performance mode". You should observe that the Instructions per Cycle (IPC) is one. This is to be expected since the processor you are evaluating is an unpipelined processor with no stalls.

The following makefile target will build all of the test programs, run them on the processor simulator, and output a summary of the results.

```
% make run
```

Review

The following sequence of commands will setup the CS250 toolflow and the RISC-V toolchain, checkout the RISC-V v1 processor example, build local RISC-V test assembly programs, build the simulator, run all assembly tests, and report the results.

```
% source ~cs250/tools/cs250.bashrc
% mkdir tut4
% cd tut4
% TUTROOT=$PWD
% cp -R ~cs250/examples/v-riscv-v1-1stage/* $TUTROOT
% cd $TUTROOT/riscv-tests
% make
% make run
% cd $TUTROOT/build/vcs-sim-rtl
% make
% make run
```

Acknowledgements

Many people have contributed to versions of this tutorial over the years. The tutorial was originally developed for CS250 VLSI Systems Design course at University of California at Berkeley by Yunsup Lee. Contributors include: Krste Asanović, Christopher Batten, John Lazzaro, and John Wawrzynek. Versions of this tutorial have been used in the following courses:

- CS250 VLSI Systems Design (2009-2010) - University of California at Berkeley
- 6.375 Complex Digital Systems (2005-2009) - Massachusetts Institute of Technology
- CSE291 Manycore System Design (2009) - University of California at San Diego