Last Time in Lecture 10

Memory Systems
- DRAM design/packaging
- Uniprocessor cache design
  - Capacity, associativity, line size
  - 3 C’s: Compulsory, Capacity, Conflict
- Multilevel caches
- Prefetching
Use snoopy mechanism to keep all processors’ view of memory coherent
Snoopy Cache, *Goodman 1983*

- Idea: Have cache watch (or snoop upon) other memory transactions, and then “do the right thing”
- Snoopy cache tags are dual-ported
Snoopy Cache Coherence Protocols

- **Write miss:**
  - the address is invalidated in all other caches before the write is performed

- **Read miss:**
  - if a dirty copy is found in some cache, a write-back is performed before the memory is read
Each cache line has state bits:

- **M**: Modified
- **S**: Shared
- **I**: Invalid

Address tag

- State bits

### Transition Diagram

- **Write miss** (P1 gets line from memory)
- **Other processor reads** (P1 writes back)
- **P1 intent to write**
- **Other processor intent to write** (P1 writes back)
- **P1 reads or writes**

- **Read miss** (P1 gets line from memory)
- **Read by any processor**

Cache state in processor P1
Two Processor Example
(Reading and writing the same cache line)

\[ \begin{align*}
P_1 \text{ reads} & \quad P_1 \text{ writes} \quad P_2 \text{ reads} \quad P_2 \text{ writes} \\
P_2 \text{ reads} & \quad P_1 \text{ writes} \quad P_1 \text{ reads} \quad P_2 \text{ writes} \quad P_1 \text{ writes} \end{align*} \]
Observation

- If a line is in the **M** state then no other cache can have a copy of the line!
- Memory stays coherent, multiple differing copies cannot exist
MESI: An Enhanced MSI protocol
increased performance for private data

Each cache line has a tag

<table>
<thead>
<tr>
<th>State</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>M</td>
<td>Modified Exclusive</td>
</tr>
<tr>
<td>E</td>
<td>Exclusive but unmodified</td>
</tr>
<tr>
<td>S</td>
<td>Shared</td>
</tr>
<tr>
<td>I</td>
<td>Invalid</td>
</tr>
</tbody>
</table>

Address tag

- Write miss
- P₁ write or read
- Other processor reads
  - P₁ writes back
- Read miss, shared
- Read by any processor
- Other processor intent to write
  - P₁ writes back
- Cache state in processor P₁

P₁ write

P₁ read

Read miss, not shared

Other processor intent to write

Other processor reads

Other processor intent to write, P₁ writes back

M: Modified Exclusive
E: Exclusive but unmodified
S: Shared
I: Invalid
Optimized Snoop with Level-2 Caches

- Processors often have two-level caches
  - small L1, large L2 (usually both on chip now)
- Inclusion property: entries in L1 must be in L2
  - invalidation in L2 $\Rightarrow$ invalidation in L1
- Snooping on L2 does not affect CPU-L1 bandwidth
When a read-miss for A occurs in cache-2, a read request for A is placed on the bus

- Cache-1 needs to supply & change its state to shared
- The memory may respond to the request also!

Does memory know it has stale data?

Cache-1 needs to intervene through memory controller to supply correct data to cache-2
False Sharing

| state | line addr | data0 | data1 | ... | dataN |

A cache line contains more than one word

Cache-coherence is done at the line-level and not word-level

Suppose $M_1$ writes $\text{word}_i$ and $M_2$ writes $\text{word}_k$ and both words have the same line address.

What can happen?
Performance of Symmetric Multiprocessors (SMPs)

Cache performance is combination of:

- Uniprocessor cache miss traffic
- Traffic caused by communication
  - Results in invalidations and subsequent cache misses
- Coherence misses
  - Sometimes called a Communication miss
  - 4th C of cache misses along with Compulsory, Capacity, & Conflict.
Coherency Misses

- True sharing misses arise from the communication of data through the cache coherence mechanism
  - Invalidates due to 1st write to shared line
  - Reads by another CPU of modified line in different cache
  - Miss would still occur if line size were 1 word

- False sharing misses when a line is invalidated because some word in the line, other than the one being read, is written into
  - Invalidation does not cause a new value to be communicated, but only causes an extra cache miss
  - Line is shared, but no word in line is actually shared
    \[ \Rightarrow \text{miss would not occur if line size were 1 word} \]
Example: True v. False Sharing v. Hit?

• Assume x1 and x2 in same cache line. P1 and P2 both read x1 and x2 before.

<table>
<thead>
<tr>
<th>Time</th>
<th>P1</th>
<th>P2</th>
<th>True, False, Hit? Why?</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Write x1</td>
<td></td>
<td>True miss; invalidate x1 in P2</td>
</tr>
<tr>
<td>2</td>
<td></td>
<td>Read x2</td>
<td>False miss; x1 irrelevant to P2</td>
</tr>
<tr>
<td>3</td>
<td>Write x1</td>
<td></td>
<td>False miss; x1 irrelevant to P2</td>
</tr>
<tr>
<td>4</td>
<td></td>
<td>Write x2</td>
<td>True miss; x2 not writeable</td>
</tr>
<tr>
<td>5</td>
<td>Read x2</td>
<td></td>
<td>True miss; invalidate x2 in P1</td>
</tr>
</tbody>
</table>
MP Performance 4-Processor Commercial Workload: OLTP, Decision Support (Database), Search Engine

- Uniprocessor cache misses improve with cache size increase (Instruction, Capacity/Conflict, Compulsory)

- True sharing and false sharing unchanged going from 1 MB to 8 MB (L3 cache)

<table>
<thead>
<tr>
<th>Cache size</th>
<th>1 MB</th>
<th>2 MB</th>
<th>4 MB</th>
<th>8 MB</th>
</tr>
</thead>
<tbody>
<tr>
<td>Instruction</td>
<td>3.25</td>
<td>1.75</td>
<td>1.50</td>
<td>1.25</td>
</tr>
<tr>
<td>Capacity/Conflict</td>
<td>2.50</td>
<td>1.50</td>
<td>1.25</td>
<td>1.00</td>
</tr>
<tr>
<td>False Sharing</td>
<td>0.75</td>
<td>0.50</td>
<td>0.50</td>
<td>0.50</td>
</tr>
<tr>
<td>True Sharing</td>
<td>0.25</td>
<td>0.25</td>
<td>0.25</td>
<td>0.25</td>
</tr>
</tbody>
</table>

Memory cycles per instruction

- Instruction
- Capacity/Conflict
- Cold
- False Sharing
- True Sharing
MP Performance 2MB Cache Commercial Workload: OLTP, Decision Support (Database), Search Engine

- True sharing, false sharing increase going from 1 to 8 CPUs
Scaling Snoopy/Broadcast Coherence

- When any processor gets a miss, must probe every other cache
- Scaling up to more processors limited by:
  - Communication bandwidth over bus
  - Snoop bandwidth into tags
- Can improve bandwidth by using multiple interleaved buses with interleaved tag banks
  - E.g., two bits of address pick which of four buses and four tag banks to use – (e.g., bits 7:6 of address pick bus/tag bank, bits 5:0 pick byte in 64-byte line)
- Buses don’t scale to large number of connections, so can use point-to-point network for larger number of nodes, but then limited by tag bandwidth when broadcasting snoop requests.
- **Insight**: Most snoops fail to find a match!
Scalable Approach: Directories

- Every memory line has associated directory information
  - keeps track of copies of cached lines and their states
  - on a miss, find directory entry, look it up, and communicate only with the nodes that have copies if necessary
  - in scalable networks, communication with directory and copies is through network transactions

- Many alternatives for organizing directory information
Assumptions: Reliable network, FIFO message delivery between any given source-destination pair
Cache States

- For each cache line, there are 4 possible states:
  - C-invalid (= Nothing): The accessed data is not resident in the cache.
  - C-shared (= Sh): The accessed data is resident in the cache, and possibly also cached at other sites. The data in memory is valid.
  - C-modified (= Ex): The accessed data is exclusively resident in this cache, and has been modified. Memory does not have the most up-to-date data.
  - C-transient (= Pending): The accessed data is in a transient state (for example, the site has just issued a protocol request, but has not received the corresponding protocol reply).
Home directory states

- For each memory line, there are 4 possible states:
  - R(dir): The memory line is shared by the sites specified in dir (dir is a set of sites). The data in memory is valid in this state. If dir is empty (i.e., dir = ε), the memory line is not cached by any site.
  - W(id): The memory line is exclusively cached at site id, and has been modified at that site. Memory does not have the most up-to-date data.
  - TR(dir): The memory line is in a transient state waiting for the acknowledgements to the invalidation requests that the home site has issued.
  - TW(id): The memory line is in a transient state waiting for a line exclusively cached at site id (i.e., in C-modified state) to make the memory line at the home site up-to-date.
Read miss, to uncached or shared line

1. Load request at head of CPU->Cache queue.
2. Load misses in cache.
3. Send ShReq message to directory.
4. Message received at directory controller.
5. Access state and directory for line. Line’s state is R, with zero or more sharers.
6. Update directory by setting bit for new processor sharer.
7. Send ShRep message with contents of cache line.
8. ShRep arrives at cache.
9. Update cache tag and data and return load data to CPU.

Interconnection Network
Write miss, to read shared line

1. Store request at head of CPU->Cache queue.
2. Store misses in cache.
3. Send ExReq message to directory.

ExReq message received at directory controller.

5. Access state and directory for line. Line’s state is R, with some set of sharers.

4. When no more sharers, send ExRep to cache.
6. Send one InvReq message to each sharer.

7. InvReq arrives at cache.
8. Invalidate cache line. Send InvRep to directory.
10. Update cache tag and data, then store data from CPU
11. ExRep arrives at cache
12. Multiple sharers
Concurrency Management

- Protocol would be easy to design if only one transaction in flight across entire system
- But, want greater throughput and don’t want to have to coordinate across entire system
- Great complexity in managing multiple outstanding concurrent transactions to cache lines
  - Can have multiple requests in flight to same cache line!
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