CS294-48 Show & Tell
Fixed-Function Graphics Pipeline
(Circa 1999)

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Hardware-Accelerated DirectX 8.1
NVIDIA GForce3 Block Diagram

AGP 8x

Cache controller & 5 channels Crossbar & 4 channel Memory Controller

Texture and Geometry Caches

128 bit DDR II Local Memory

8 Texture Fetch & Filtering & Decompression Units

Vertex Processing

Vertex Processing

Texture and Fragment Processing

Color & Z compression decompression

Z-Compare and Blend

Host

Cell / Clip / Setup

Rasterization

Texture Cache

Fragment Crossbar

Memory Partition

Memory Partition

Memory Partition

Memory Partition

DRAM(s)

DRAM(s)

DRAM(s)

DRAM(s)

2 CRT& Interfaces: 2xRAMDAC, 1xTV, 3xTDMS

2D Core

Color & Z Tile Cache for Frame Buffer data

MSAA Allocation

FSAA Post-processor

Tile HSR Logic

Frame Buffer Logic

3 Vertex Processors

8 Texture & 2 Color 4D Interpolators

8 Pixel Processors

VGA

TV

DVI
Highlights

• Only “Fixed-Function Pipeline” considered
• An embarrassingly data-parallel problem.
• A sequence of several SIMD stages
• A modified memory hierarchy (special texture ops)
• Striped access to off-chip memory

• Difficult to find representative block diagrams of modern ICs - helps to go back a decade.