

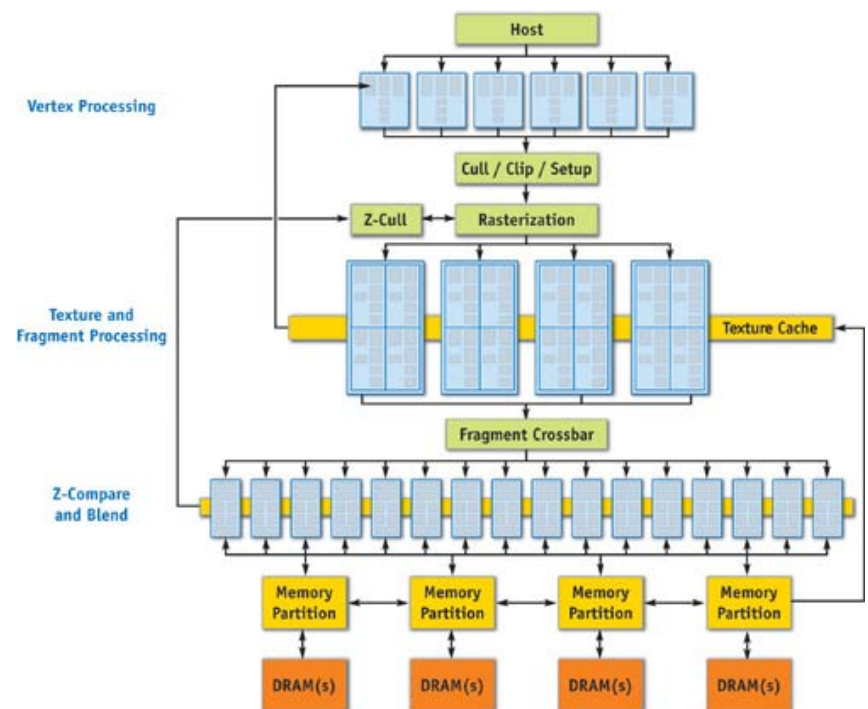
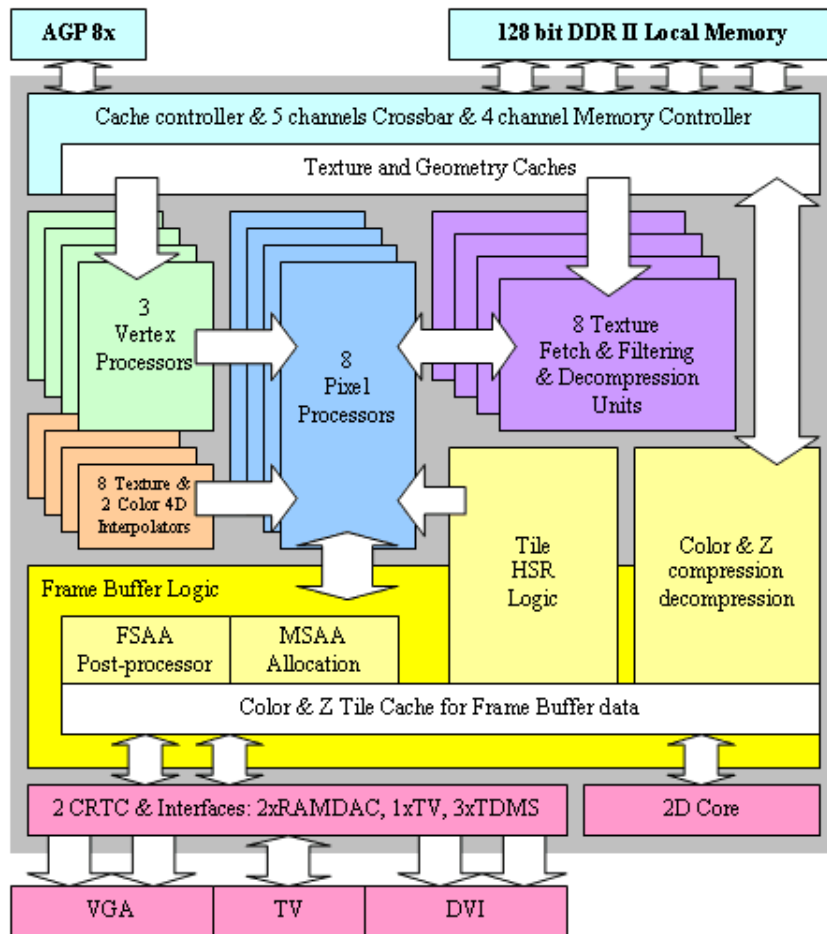
CS294-48 Show & Tell  
Fixed-Function Graphics Pipeline  
(Circa 1999)

Ilia Lebedev

The diagram illustrates a comprehensive graphics pipeline, organized into several key stages:

- Vertex Declaration & Shader Declaration:** The initial input stage, providing vertex data (v0-v15) and shader data (r0-r11).
- Vertex Shader ALU & Shader Function:** Processes vertex data and shader instructions, outputting a0-a7, c0-c7, and i.
- Vertex Assembly:** Combines data from Matrix Palette, World Matrices (0-3), Vertex Blend, View Matrix, Texture Coordinate Generation, Vertex Flag, Lighting, and Projection Matrix.
- Primitive Assembly:** Performs Face Culling, User Clip Planes, Frustum Clipping, Homogeneous Divide, and Viewport Mapping.
- Pixel Shader ALU & Shader Function:** Processes pixel data through Input Registers, Component Multiplex, Scale/Offset, and Component Mask, outputting r0-r11 and a0-a7.
- Texture Stage:** Manages Color Arg (0-3), Alpha Arg (0-2), and various texture operations like Color Op, Alpha Op, and Texture Op.
- Rasterization and Component Interpolation:** Handles Texture Addressing, Texture Sampling, and Texture Stages (0-7).
- Fog Blend:** Includes Alpha Test, Depth Test, Stencil Test, Alpha Blend, and Render Target.
- Device Resources:** Manages Index Buffer, Vertex Buffer, Volume Texture, Surface Texture, and Cube Texture.
- Presentation:** The final output stage, including Video Scanout, Cursor, Gamma Ramp, DDA Converter, and CRT Monitor.

# NVIDIA GForce3 Block Diagram



# Highlights

- Only “Fixed-Function Pipeline” considered
  - An embarrassingly data-parallel problem.
  - A sequence of several SIMD stages
  - A modified memory hierarchy (special texture ops)
  - Striped access to off-chip memory
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- Difficult to find representative block diagrams of modern ICs - helps to go back a decade.