Pattern Decomposition of Fulcrum’s Focal Point II
(24 Port x 10GigE Network Switch Chip)

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Context
Overview

- Objectives
  - 24 x 10 GigE (up to 240 Gbps) at 200ns and 360Mpps
  - Want to switch at L2/L3, and track data for L2-L4
  - General enough to be ASIC sold on multiple platforms
- Many patterns present
General Pipeline
Fabricated in TSMC 0.13um
250 Million Transistors
FP II L2-L4 Packet Processing Pipeline

- Status From Scheduler
- Inter-Frame Switch State Update
  - Statistics
  - QoS State
  - Learning / Aging

24 Ports → Merge FIFO → Unified LPM / ACL CAM

- 72KB TCAM
  - L3 LPM Lookup
  - L2/L3/L4 ACL
  - Soft-config Key Pattern VRRP

- 16K-entry ARP Cache
  - Per VLAN default Routes
  - 16 Way ECMP

ARP Table → L2 VLAN / STP Table

- 4K VLANs
- 4K Spanning Trees

MAC Table → Stacking TAG Table

- 16K entries
  - Unified unicast / multicast

LAG QoS Triggers → Port Mask To Scheduler

CAM-based ISL Table → Discard
Patterns

- Machine Organization: Heterogeneous MCMD Distributed Memory
  - At the highest level, distributed memory (SRAM, TCAM)
  - Multiple agents of different types can share a type of memory
- Processing: In-order pipeline or FSM
- Memory: Many banks/ports to allow high concurrency, writes decoupled
- Switch: Crossbar or multi-stage
- Hardware Building Blocks: Large system, most patterns used