CS294-48: Hardware Design Patterns
Meeting 2: BHPL Version 0.2

Krste Asanovic
UC Berkeley
Fall 2009
Course Overview

MP3 bit string

Application(s)

(Berkeley) Hardware Pattern Language

MP3 bit string

Hardware (RTL)

Audio
BHPL Version 0.1

**Application Patterns (from OPL)**
- Structural Patterns
  - Pipelines
  - Agent&Repository
  - Model-View-Controller
  - Event Based
  - Process Control
  - Iteration
  - Map-Reduce
  - Layered Systems
  - Task Graphs

**Computational Patterns**
- Circuits
- Dense Linear Algebra
- N-Body Methods
- Sparse Linear Algebra
- Spectral Methods
- Unstructured Grids
- Graph Traversal
- Structured Grids
- Graph Algorithms
- FSMs
- Dynamic Programming

**Machine Organizations**
- Systolic
- SIMD Shared Memory
- SIMD Distributed Memory
- MIMD Shared Memory
- Homogeneous MIMD Distributed Memory
- Heterogeneous MIMD Distributed Memory

**Processing**
- In-Order Pipeline
- Out-of-Order Pipeline

**Memory**
- Banked Memory
- Bypassed Memory
- Cached Memory

**Switch**
- Bus
- Crossbar
- Multi-Stage Networks

**Hardware Building Blocks**
- FIFO
- Multiport Memory
- CAM
- Arbiter
- Communication Channel

**PMS Layer**
- Microcoded Engine
- Threaded Pipeline

**FSM**

**Structural Patterns**
- In-Order Pipeline

**Structured Patterns**
- Model-View-Controller
- Event Based
- Process Control
- Iteration
- Map-Reduce
- Layered Systems
- Task Graphs

**Computational Patterns**
- Circuits
- Dense Linear Algebra
- N-Body Methods
- Sparse Linear Algebra
- Spectral Methods
- Unstructured Grids
- Graph Traversal
- Structured Grids
- Graph Algorithms
- FSMs
- Dynamic Programming
From Last Time

- Taxonomy plus patterns, not just patterns
- Different types of pattern at each level
  - Mapping from motif to machine organization
  - Mapping of control stream execution needs to pipeline design
- Make less processor-centric
Structural Taxonomy Components

- Controllers
- Datapaths
- Memories
- Networks
Machine Organizations

- Describes overall structure of machine
- Can be composed hierarchically
- Some Important dimensions:
  - SCMD versus MCMD
  - Distributed versus shared memory between datapaths
- Systolic?
SCMD Distributed Memory

Examples: MPP, ICL DAP, CM-1, CM-2, MasPar, Sony Playstation-2 Graphics Engine, Vision processing chips
SCMD Shared Memory

Examples: STARAN, BSP, TI ASC, CDC
Star-100, Multi-Lane Vector Machines
MCMD Shared Memory

- Examples: Burroughs B5x00 series, Network Packet Routers
Homogeneous MCMD
Distributed Memory

- Examples: Caltech Cosmic Cube, Transputer, nCube, Clusters
Heterogeneous MCMD
Distributed Memory

\[ P = C + D \]

- Examples: Signal Processing Pipelines,
Systolic

\[ P = C + D \]

- Examples: Warp, Raw, Motion Estimation Engines,
Controller Types

- **State Machine Controller**
  - control lines generated by state machine

- **Microcoded Controller**
  - single-cycle datapath, control lines in ROM/RAM

- **In-Order Pipeline Controller**
  - pipelined control, dynamic interaction between stages

- **Out-of-Order Pipeline Controller**
  - operations within a control stream might be reordered internally

- **Threaded Pipeline Controller**
  - multiple control streams one execution pipeline
  - can be either in-order (PPU) or out-of-order
Memory Structures

- **True Multiport Memory**
- **Banked Memory**
  - Interleave lesser-ported banks to provide higher bandwidth
- **Cached Memory**
  - Memory hierarchy to provide higher-bandwidth, lower latency for predictable accesses
- **Bypassed Memory**
  - Reduce latency of pipelined dependent memory accesses
Switches

- Connects multiple agents (processors and/or memories)
- Bus
  - Low-cost, ordered
- Crossbar
  - High-performance
- Multi-stage network
  - Trade cost/performance
Connectors

- How one structural component connects to another

- Control -> Datapath
  - direct
  - pipelined? (maybe don’t need pipelined controller?)

- Datapath <-> Memory
  - fixed latency
  - cannot have shared memory without true multiport
  - decoupled in-order
  - out-of-order

- Control <-> Network <-> Control
  - fixed latency
  - FIFOs
  - addressable messaging