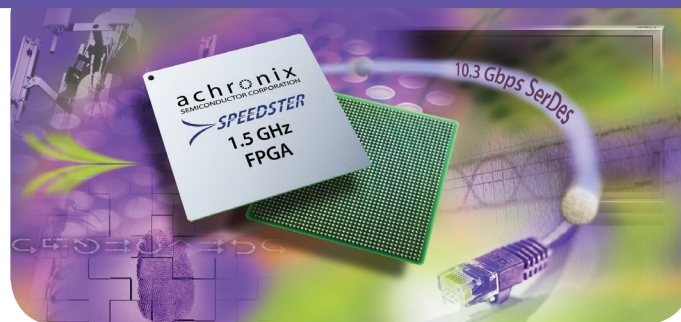


PRODUCT BRIEF

Speedster® FPGA Family

SPEEDSTER HIGHLIGHTS

- Fastest FPGA family in the world:
 - 1.5 GHz system performance
 - SRAM-based FPGAs
 - Field reprogrammable
- Logic capacity up to 1.5 Million ASIC gates
- 18Kb RAM blocks
- Up to 40 lanes of embedded 10.3 Gbps SerDes
- 10.3 Gbps SerDes supporting high-speed serial interfaces including:
 - PCI-Express
 - Gigabit Ethernet
 - CEI-6G
 - 10 Gbps Backplane
 - XAUI
 - XFI
 - Infiniband
- Industry standard Memory interfaces supported:
 - SDR SDRAM (200 Mbps)
 - QDR SRAM (400 Mbps)
 - QDRII SRAM (800 Mbps)
 - RLDRAM II (1066 Mbps)
 - DDR1 SDRAM (400 Mbps)
 - DDR2 SDRAM (800 Mbps)
 - DDR3 SDRAM (1066 Mbps)
- Industry standard datapath interfaces supported:
 - SPI-4.2 (Up to 1000 Mbps)
 - SFI-4.1 (622 Mbps)
 - XSBI (644 Mbps)
- Standard RTL synthesis design entry using either
 - Synplify Pro from Synopsis or
 - Precision Synthesis from Mentor Graphics
- Achronix CAD Environment (ACE) tools provide back-end implementation
- Performance can be traded off for:
 - Lower power consumption through voltage scaling
 - Higher effective capacity
- Rapid timing closure yields significant time-to-market advantages
- Based on proven TSMC 65 nm CMOS process



The Speedster family of Field Programmable Gate Arrays (FPGAs) from Achronix Semiconductor are the world's fastest programmable logic devices. Speedster FPGAs are fully reprogrammable, yet still capable of operating at up to 1.5 GHz system performance. The Speedster FPGA family is suitable for a wide range of telecommunications, networking, video, digital signal processing, high-performance computing, imaging, industrial and military applications.

Unprecedented FPGA Performance

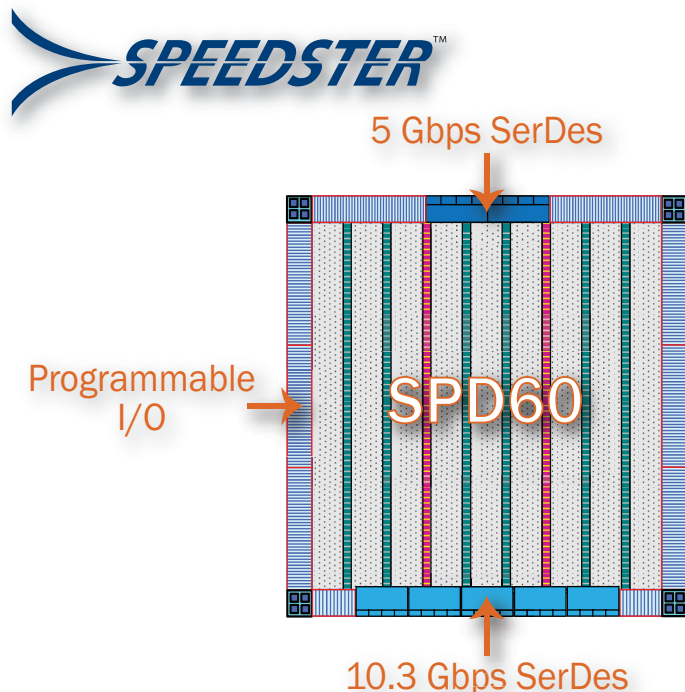
The Speedster family removes system performance barriers associated with conventional FPGAs. Achieving system speeds of up to 1.5 GHz, the Speedster family delivers the only FPGAs in the world capable of exceeding standard cell ASIC performance. This unprecedented performance, coupled with the flexibility of a reprogrammable solution, makes Speedster FPGAs ideal for applications requiring high data throughput. With Speedster FPGAs, designers no longer need to compromise performance to benefit from the flexibility of an FPGA. Speedster FPGAs provide designers a disruptive but familiar platform for implementing their highest performance designs while avoiding high ASIC cost and timing closure problems that plague other FPGAs. Achronix™ Speedster FPGAs are general purpose, allowing a wide range of applications to achieve high performance without requiring RTL customization or manual optimization. The Speedster FPGA architecture employs a regular array of Reconfigurable Logic Blocks (RLBs) connected through a programmable interconnect. Each RLB contains eight 4-input LUTs, and can also be configured as 128 bits of 1.5 GHz distributed RAM.

The Speedster family also contains dedicated 18×18 multipliers capable of GHz performance. The high performance interconnect allows the multipliers to be combined with LUT-based adders, accumulators and other functions to build DSP functions.

The unique technology used to build the Achronix logic fabric removes the limit on the number of internal clock networks. Therefore, Speedster FPGAs can be used to implement designs with a high number of clock domains, a capability available only in ASICs before now.

High-Speed Interfaces

To complement the 1.5 GHz logic fabric, Speedster FPGAs are equipped with numerous programmable high-speed SerDes channels and highly flexible, programmable I/O. With up to 40 SerDes lanes and an additional 933 high-speed programmable I/Os the Speedster family provides high I/O bandwidth to match the internal logic performance. The combination of I/Os, SerDes memory and logic performance makes Speedster devices suitable for numerous high-bandwidth protocols such as PCI Express, CEI-6G, 10 Gbps Ethernet, etc.



Speedster Product Family

DEVICE NAME	SPD30	SPD60	SPD100	SPD180
Number of LUTs	24,576	47,040	93,848	163,840
picoPIPE Pipeline Elements	1,725,000	3,400,000	7,200,000	11,700,000
Number of 18Kbit Block RAM	66	144	334	556
Available Block RAM (Kbit)	1188	2592	6012	10008
Available Distributed RAM (Kbit)	384	735	1232	2560
Number of Multipliers (18×18)	50	98	120	270
Number of 5 Gbps SerDes Lanes	-	8	-	-
Number of 10.3 Gbps SerDes Lanes	8	20	36	40
DDR3/DDR2 Controller (1066 Mbps)	2	4	4	4
Number of PLLs	8	16	16	16
User Programmable I/Os†	488	792	832	933
FBGA899 31×31‡	514	-	-	-
FBGA1285 37.5×37.5‡	520	712	722	-
FBGA1892 45×45‡	-	918	976	1010

† Pin counts include user data and user clock, but not SerDes signals.

‡ Pin counts include SerDes signals

Design Methodology

The Achronix implementation flow uses an industry standard RTL synthesis flow based on Synplify Pro from Synopsis (formerly Synplicity) and Precision Synthesis from Mentor Graphics. Working in conjunction with the synthesis tool, the Achronix CAD Environment (ACE) provides placement, routing, timing analysis, bitstream generation and FPGA configuration.

Simulation is supported using industry standard simulators, and on-chip debug access allows further verification capability.

For product development, a standard JTAG interface can be used to program Speedster FPGAs. In a production environment, configuration via SPI flash is available. Additionally, the device can be programmed using an external CPU. For security, Speedster FPGAs include an integrated 256-bit AES encryption engine for bitstream protection.

Trading Performance for Power

Speedster devices have a unique ability for robust operation over a wide range of supply voltages. This allows the core voltage to be reduced to a level that ensures performance requirements are met, while achieving optimal power consumption. As there is a V^2f relationship between power consumption and voltage, a small reduction in core voltage results in a large reduction in power consumption.

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