Set Associative Caches

Indices represent sets of associative cache blocks, which use a replacement strategy when the bucket is full.

**Problems**

1. How big should the T, I, and O fields of a memory address be on a system with...?
   a. 32-bit addressed memory, 64 KB fully associative cache, 4-byte blocks
   b. 32-bit addressed memory, 64 KB fully associative cache, 16-byte blocks
   c. 8-bit addressed memory, 32 B 2-way set associative cache, 4-byte blocks
   d. 8-bit addressed memory, 32 B 4-way set associative cache, 4-byte blocks
Practice Question (From Su 98, Question 4)

1. A 32kB cache has a linesize of 16 bytes and is 4-way set-associative. How many bits of an address will be in the Tag, Index, and Offset?

2. In a 2-way set-associative cache, three addresses, A, B, and C, all have the same index but distinct tags. What is a minimum sequence of accesses which, if repeated, will maximize the miss rate in the cache if it uses the LRU replacement policy?

3. If the above sequence is repeated for a long period of time, what will the miss rate be if the cache uses an LRU replacement policy?

4. If the hit time is 1 cycle, and the miss penalty is 3 cycles, what will be the average memory access time (in clock cycles) for the LRU replacement policy using the above sequence?

5. If the sequence is repeated for a long period of time, will the miss rate be improved if random is used as the replacement policy?

6. What will the miss rate be for LRU replacement when the sequence is A B C C B A A B C . . . ?