Memory Mapped I/O

Certain memory addresses correspond to registers in I/O devices and not normal memory.

**Control Register:** Indicates if it is okay to read/write data register

**Data Register:** Contains I/O data

<table>
<thead>
<tr>
<th>Register</th>
<th>Location</th>
<th>Contains</th>
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<tbody>
<tr>
<td>Receiver Control</td>
<td>0xffff0000</td>
<td>Lowest two bits: Interrupt Enable Bit, Ready Bit</td>
</tr>
<tr>
<td>Receiver Data</td>
<td>0xffff0004</td>
<td>Received data stored at lowest byte</td>
</tr>
<tr>
<td>Transmitter Control</td>
<td>0xffff0008</td>
<td>Lowest two bits: Interrupt Enable Bit, Ready Bit</td>
</tr>
<tr>
<td>Transmitter Data</td>
<td>0xffff000c</td>
<td>Transmitted data stored at lowest byte</td>
</tr>
</tbody>
</table>

Write MIPS code to read a byte from the receiver and immediately send it to the transmitter.

Polling and Interrupts

<table>
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<th>Operation</th>
<th>Definition</th>
<th>Pro/Con</th>
<th>Good For</th>
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<tr>
<td>Polling</td>
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Interrupt Enable: Indicates whether or not to cause an interrupt when the ready bit is set
Network Overhead vs. Bandwidth
Assume we have two networks A and B.
   Network A has a 200us overhead and a peak bandwidth of 10MB/s
   Network B has a 500us overhead and a peak bandwidth of 100MB/s
   (MB = MegaByte)

How long would it take to send 1000 Bytes over each network?
Which network is better for sending large amounts of data?

AMAT
Suppose:
   • L1 access is 2 cycles.
   • L2 access is 4 cycles.
   • Suppose a 95% hit rate in L1 for data, and a global 99% hit rate in L2 for data.
   • Main memory is 100 cycles.
   • Page table lookup is 150 cycles
   • L1 and L2 both are physically tagged.
   • A 99% TLB hit rate. TLB lookup can be parallelized with memory access, so a TLB hit is effectively free.
   • Ignore effects of having page table entries in data cache.

What is the AMAT for data?

What if we disabled virtual memory?

Now let's suppose one time in five million we have a page fault and it takes 10 million cycles to service. What happens to AMAT?