CS 61C: Great Ideas in Computer Architecture

Instruction Level Parallelism: Multiple Instruction Issue

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Review

The BIG Picture

- Pipelining improves performance by increasing instruction throughput: exploits ILP
  - Executes multiple instructions in parallel
  - Each instruction has the same latency
- Subject to hazards
  - Structure, data, control
- Stalls reduce performance
  - But are required to get correct results
- Compiler can arrange code to avoid hazards and stalls
  - Requires knowledge of the pipeline structure

Agenda

- More ILP
- Instruction Scheduling
- Administrivia
- Out of Order Execution
- Parallelism Big Picture
- And, in Conclusion, ...

Greater Instruction-Level Parallelism (ILP)

- Deeper pipeline (5 => 10 => 15 stages)
  - Less work per stage ⇒ shorter clock cycle
- Multiple issue “superscalar”
  - Replicate pipeline stages ⇒ multiple pipelines
  - Start multiple instructions per clock cycle
  - CPI < 1, so use Instructions Per Cycle (IPC)
  - E.g., 4GHz 4-way multiple-issue
    - 16 BIPS, peak CPI = 0.25, peak IPC = 4
  - But dependencies reduce this in practice

You Are Here!

- Parallel Requests Assigned to computer e.g., Search “Katz”
- Parallel Threads Assigned to core e.g., Lookup, Ads
- Parallel Instructions >1 instruction @ one time e.g., 5 pipelined instructions
- Parallel Data >1 data item @ one time e.g., Add of 4 pairs of words
- Hardware descriptions All gates @ one time
- Programming Languages

Agenda
Multiple Issue

- Static multiple issue
  - Compiler groups instructions to be issued together
  - Packages them into “issue slots”
  - Compiler detects and avoids hazards
- Dynamic multiple issue
  - CPU examines instruction stream and chooses instructions to issue each cycle
  - Compiler can help by reordering instructions
  - CPU resolves hazards using advanced techniques at runtime

Pipeline Depth and Issue Width

- Intel Processors over Time

<table>
<thead>
<tr>
<th>Microprocessor</th>
<th>Year</th>
<th>Clock Rate</th>
<th>Pipeline Stages</th>
<th>Issue width</th>
<th>Cores</th>
<th>Power</th>
</tr>
</thead>
<tbody>
<tr>
<td>486</td>
<td>1989</td>
<td>25 MHz</td>
<td>5</td>
<td>1</td>
<td>1</td>
<td>5W</td>
</tr>
<tr>
<td>Pentium</td>
<td>1993</td>
<td>66 MHz</td>
<td>5</td>
<td>2</td>
<td>1</td>
<td>10W</td>
</tr>
<tr>
<td>Pentium Pro</td>
<td>1997</td>
<td>200 MHz</td>
<td>10</td>
<td>1</td>
<td>1</td>
<td>29W</td>
</tr>
<tr>
<td>P4 Willamette</td>
<td>2001</td>
<td>2000 MHz</td>
<td>22</td>
<td>3</td>
<td>1</td>
<td>75W</td>
</tr>
<tr>
<td>P4 Prescott</td>
<td>2004</td>
<td>3600 MHz</td>
<td>31</td>
<td>3</td>
<td>1</td>
<td>103W</td>
</tr>
<tr>
<td>Core 2 Conroe</td>
<td>2006</td>
<td>2930 MHz</td>
<td>14</td>
<td>4</td>
<td>2</td>
<td>75W</td>
</tr>
<tr>
<td>Core 2 Yorkfield</td>
<td>2008</td>
<td>2930 MHz</td>
<td>16</td>
<td>4</td>
<td>4</td>
<td>96W</td>
</tr>
<tr>
<td>Core i7 Guilford</td>
<td>2012</td>
<td>3460 MHz</td>
<td>16</td>
<td>4</td>
<td>6</td>
<td>130W</td>
</tr>
</tbody>
</table>

Static Multiple Issue

- Compiler groups instructions into “issue packets”
  - Group of instructions that can be issued on a single cycle
  - Determined by pipeline resources required
- Think of an issue packet as a very long instruction
  - Specifies multiple concurrent operations

Scheduling Static Multiple Issue

- Compiler must remove some/all hazards
  - Reorder instructions into issue packets
  - No dependencies with a packet
  - Possibly some dependencies between packets
    - Varies between ISAs; compiler must know!
    - Pad with nop if necessary
MIPS with Static Dual Issue

- Two-issue packets
  - One ALU/branch instruction
  - One load/store instruction
  - 64-bit aligned
  - ALU/branch, then load/store
  - Pad an unused instruction with nop

<table>
<thead>
<tr>
<th>Address</th>
<th>Instruction type</th>
<th>Pipeline Stages</th>
</tr>
</thead>
<tbody>
<tr>
<td>n</td>
<td>ALU/branch</td>
<td>IF ID EX MEM WB</td>
</tr>
<tr>
<td>n + 4</td>
<td>Load/store</td>
<td>IF ID EX MEM WB</td>
</tr>
<tr>
<td>n + 8</td>
<td>ALU/branch</td>
<td>IF ID EX MEM WB</td>
</tr>
<tr>
<td>n + 12</td>
<td>Load/store</td>
<td>IF ID EX MEM WB</td>
</tr>
<tr>
<td>n + 16</td>
<td>ALU/branch</td>
<td>IF ID EX MEM WB</td>
</tr>
<tr>
<td>n + 20</td>
<td>Load/store</td>
<td>IF ID EX MEM WB</td>
</tr>
</tbody>
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Hazards in the Dual-Issue MIPS

- More instructions executing in parallel
- EX data hazard
  - Forwarding avoided stalls with single-issue
  - Now can’t use ALU result in load/store in same packet
    - add $t0, $s0, $s1
      - load $s2, 0($t0)
    - Split into two packets, effectively a stall
- Load-use hazard
  - Still one cycle use latency, but now two instructions
- More aggressive scheduling required

Scheduling Example

- Schedule this for dual-issue MIPS

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<td>loop</td>
<td>ALU/branch</td>
<td>IF ID EX MEM WB</td>
</tr>
<tr>
<td>addi</td>
<td>ALU/branch</td>
<td>IF ID EX MEM WB</td>
</tr>
<tr>
<td>bne</td>
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- IPC = 5/4 = 1.25 (c.f. peak IPC = 2)

Loop Unrolling

- Replicate loop body to expose more parallelism
  - Reduces loop-control overhead
- Use different registers per replication
  - Called “register renaming”
  - Avoid loop-carried “anti-dependencies”
    - Store followed by a load of the same register
    - Aka “name dependence”
      - Reuse of a register name

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- IPC = 14/8 = 1.75
  - Closer to 2, but at cost of registers and code size

Loop Unrolling Example

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- “Superscalar” processors
- CPU decides whether to issue 0, 1, 2, … each cycle
  - Avoiding structural and data hazards
- Avises the need for compiler scheduling
  - Though it may still help
  - Code semantics ensured by the CPU

Dynamic Multiple Issue
Dynamic Pipeline Scheduling

- Allow the CPU to execute instructions out of order to avoid stalls
  - But commit result to registers in order

  **Example**

  ```
  lw $t0, 20($s2)
  addu $t1, $t0, $t2
  subu $s4, $s4, $t3
  slti $t5, $s4, 20
  ```

  - Can start subu while addu is waiting for lw

Why Do Dynamic Scheduling?

- Why not just let the compiler schedule code?
  - Not all stalls are predictable
  - e.g., cache misses
- Can’t always schedule around branches
  - Branch outcome is dynamically determined
- Different implementations of an ISA have different latencies and hazards

Agenda

- More ILP
- Instruction Scheduling
- Administrivia
- Out of Order Execution
- Parallelism Big Picture
- And, in Conclusion, ...

Speculation

- "Guess" what to do with an instruction
  - Start operation as soon as possible
  - Check whether guess was right
    - If so, complete the operation
    - If not, roll-back and do the right thing
- Common to static and dynamic multiple issue
- Examples
  - Speculate on branch outcome (Branch Prediction)
    - Roll back if path taken is different
    - Speculate on load
    - Roll back if location is updated

Administrivia

- As of today, made 1 pass over all Big Ideas in Computer Architecture
- Following lectures go into more depth on topics you’ve already seen while you work on projects
  - 1 lecture in more depth on Caches
  - 1 on Protection, Virtual Memory, Virtual Machines
  - 1 on Exceptions, Traps, Interrupts
  - 2 on Modern Phone and Computer Architectures
  - 1 on Programming Contest (Extra Credit Project 5)
  - 1 on Course Wrap-up and Review
Pipeline Hazard: Matching socks in later load

Out-of-Order Laundry: Don’t Wait

Out-of-Order Execution (1/2)
- Basically, unroll loops in hardware
  1. Fetch instructions in program order (≤4/clock)
  2. Predict branches as taken/untaken
  3. To avoid hazards on registers, rename registers using a set of internal registers (~80 registers)
  4. Collection of renamed instructions might execute in a window (~60 instructions)
  5. Execute instructions with ready operands in 1 of multiple functional units (ALUs, FPUs, Ld/St)

Out-of-Order Execution (2/2)
- Basically, unroll loops in hardware
  6. Buffer results of executed instructions until predicted branches are resolved in reorder buffer
  7. If predicted branch correctly, commit results in program order
  8. If predicted branch incorrectly, discard all dependent results and start with correct PC

Out Of Order Intel
- All use OOO since 2001

<table>
<thead>
<tr>
<th>Microprocessor</th>
<th>Year</th>
<th>Clock Rate</th>
<th>Pipeline Stages</th>
<th>Issue width</th>
<th>Out of order/Speculation</th>
<th>Cores</th>
<th>Power</th>
</tr>
</thead>
<tbody>
<tr>
<td>i486</td>
<td>1989</td>
<td>25MHz</td>
<td>5</td>
<td>1</td>
<td>No</td>
<td>1</td>
<td>5W</td>
</tr>
<tr>
<td>Pentium</td>
<td>1993</td>
<td>66MHz</td>
<td>5</td>
<td>2</td>
<td>No</td>
<td>1</td>
<td>10W</td>
</tr>
<tr>
<td>Pentium Pro</td>
<td>1997</td>
<td>200MHz</td>
<td>10</td>
<td>3</td>
<td>Yes</td>
<td>1</td>
<td>29W</td>
</tr>
<tr>
<td>P6 Millennium</td>
<td>2001</td>
<td>3600MHz</td>
<td>22</td>
<td>3</td>
<td>Yes</td>
<td>1</td>
<td>29W</td>
</tr>
<tr>
<td>P6 Prescott</td>
<td>2004</td>
<td>3000MHz</td>
<td>31</td>
<td>2</td>
<td>Yes</td>
<td>1</td>
<td>110W</td>
</tr>
<tr>
<td>Core</td>
<td>2005</td>
<td>2300MHz</td>
<td>14</td>
<td>4</td>
<td>Yes</td>
<td>1</td>
<td>29W</td>
</tr>
<tr>
<td>Core 2</td>
<td>2006</td>
<td>2600MHz</td>
<td>16</td>
<td>4</td>
<td>Yes</td>
<td>4</td>
<td>95W</td>
</tr>
<tr>
<td>Core 2 Goshen</td>
<td>2007</td>
<td>2040MHz</td>
<td>18</td>
<td>4</td>
<td>Yes</td>
<td>8</td>
<td>150W</td>
</tr>
</tbody>
</table>

AMD Opteron X4 Microarchitecture
AMD Opteron X4 Pipeline Flow

- For integer operations
  - 12 stages (Floating Point is 17 stages)
  - Up to 106 RISC-ops in progress
  - Intel Nehalem is 16 stages for integer operations, details not revealed, but likely similar to above+
  - Intel calls RISC operations “Micro operations” or “μops”

Does Multiple Issue Work?

**The BIG Picture**

- Yes, but not as much as we’d like
- Programs have real dependencies that limit ILP
- Some dependencies are hard to eliminate
  - e.g., pointer aliasing
- Some parallelism is hard to expose
  - Limited window size during instruction issue
- Memory delays and limited bandwidth
  - Hard to keep pipelines full
- Speculation can help if done well

Dynamically Scheduled CPU

Big Picture on Parallelism

Two types of parallelism in applications

1. **Data-Level Parallelism (DLP):** arises because there are many data items that can be operated on at the same time
2. **Task-Level Parallelism (TLP):** arises because tasks of work are created that can operate largely in parallel

Big Picture on Parallelism

Hardware can exploit app Data LP and Task LP in 4 ways:

1. **Instruction-Level Parallelism:** Hardware exploits application DLP using ideas like pipelining and speculative execution
2. **SIMD architectures:** exploit app DLP by applying a single instruction to a collection of data in parallel
3. **Thread-Level Parallelism:** exploits either app DLP or TLP in a tightly-coupled hardware model that allows for interaction among parallel threads
4. **Request-Level Parallelism:** exploits parallelism among largely decoupled tasks and is specified by the programmer of the operating system

“And in Conclusion..”

- Pipeline challenge is hazards
  - Forwarding helps w/many data hazards
  - Delayed branch helps with control hazard in 5 stage pipeline
  - Load delay slot / interlock necessary
- More aggressive performance:
  - Longer pipelines
  - Superscalar
  - Out-of-order execution
  - Speculation
State if following techniques are associated primarily with a software- or hardware-based approach to exploiting ILP (in some cases, the answer may be both): Superscalar, Out-of-Order execution, Speculation, Register Renaming

<table>
<thead>
<tr>
<th></th>
<th>Superscalar</th>
<th>Out-of-Order</th>
<th>Speculation</th>
<th>Register Renaming</th>
</tr>
</thead>
<tbody>
<tr>
<td>Orange</td>
<td>HW</td>
<td>HW</td>
<td>HW</td>
<td>HW</td>
</tr>
<tr>
<td>Green</td>
<td>HW</td>
<td>HW</td>
<td>Both</td>
<td>Both</td>
</tr>
<tr>
<td>Pink</td>
<td>HW</td>
<td>HW</td>
<td>Both</td>
<td>Both</td>
</tr>
<tr>
<td>Yellow</td>
<td>HW</td>
<td>HW</td>
<td>HW</td>
<td>SW</td>
</tr>
</tbody>
</table>

Instr LP, SIMD, Thread LP, Request LP are examples of

- Parallelism above (\(\land\)) the Instruction Set Architecture
- Parallelism explicitly at (\(\equiv\)) the level of the ISA
- Parallelism below (\(\lor\)) the level of the ISA

<table>
<thead>
<tr>
<th></th>
<th>Inst. LP</th>
<th>SIMD</th>
<th>Thr. LP</th>
<th>Req. LP</th>
</tr>
</thead>
<tbody>
<tr>
<td>Orange</td>
<td>(\lor)</td>
<td>(\equiv)</td>
<td>(\land)</td>
<td>(\land)</td>
</tr>
<tr>
<td>Green</td>
<td>(\equiv)</td>
<td>(\land)</td>
<td>(\land)</td>
<td>(\land)</td>
</tr>
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<td>(\lor)</td>
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<td>(\land)</td>
<td>(\land)</td>
</tr>
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<td>Yellow</td>
<td>(\equiv)</td>
<td>(\land)</td>
<td>(\land)</td>
<td>(\land)</td>
</tr>
</tbody>
</table>

I. Thanks to pipelining, I have reduced the time it took me to wash my one shirt.

II. Longer pipelines are always a win (since less work per stage & a faster clock).

A)[orange] I is True and II is True
B)[green] I is False and II is True
C)[pink] I is True and II is False
D)[yellow] I is False and II is False

Red I is True and II is True
Orange I is False and II is True
Green I is True and II is False
Yellow I is False and II is False
Peer Question

Not all instructions are active in every stage of the 5-stage pipeline. Ignoring the effects of hazards, which of the following is true?
1. Allowing jumps, branches, and ALU instructions to take fewer stages than the 5 required by the load instruction will increase pipeline performance for most programs.
2. You cannot make ALU instructions take fewer cycles because of the write back of the result, but branches and jumps can take fewer cycles, so there is some opportunity for improvement.
3. Instead of trying to make instructions take fewer cycles, we should explore making the pipeline longer, so that instructions take more cycles, but the cycles are shorter. This could improve performance.
4. The number of pipe stages per instruction affects throughput, not latency.

Orange: 1
Green: 2
Pink: 3
Yellow: 4

Peer Answer

Not all instructions are active in every stage of the 5-stage pipeline. Ignoring the effects of hazards, which of the following is true?
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“And in Conclusion, …”

• Big Ideas of Instruction Level Parallelism
• Pipelining, Hazards, and Stalls
• Forwarding, Speculation to overcome Hazards
• Multiple issue to increase performance
  — IPC instead of CPI
• Dynamic Execution: Superscalar in-order issue, branch prediction, register renaming, out-of-order execution, in-order commit
  — “unroll loops in HW”, hide cache misses