Recap: Adding branches to datapath

Implementing \texttt{JALR} Instruction (I-Format)

\begin{tabular}{|c|c|c|c|c|c|}
\hline
\texttt{inst} & \texttt{rs} & \texttt{func3} & \texttt{rd} & \texttt{opcode} \\
\hline
12 & 5 & 3 & 5 & 7 \\
\hline
\end{tabular}

- \texttt{JALR} \texttt{rd}, \texttt{rs}, immediate
  - Writes PC+4 to Reg[\texttt{rd}] (return address)
  - Sets PC = Reg[\texttt{rs1}] + immediate
  - Uses same immediates as arithmetic and loads
    - \texttt{no} multiplication by 2 bytes

Adding \texttt{jalr} to datapath
Implementing jal Instruction

- JAL saves PC+4 in Reg[rd] (the return address)
- Set PC = PC + offset (PC-relative jump)
- Target somewhere within ±2^{19} locations, 2 bytes apart
  - ±2^{18} 32-bit instructions
- Immediate encoding optimized similarly to branch instruction to reduce hardware cost

Adding jal to datapath

“Upper Immediate” instructions

- Has 20-bit immediate in upper 20 bits of 32-bit instruction word
- One destination register, rd
- Used for two instructions
  - LUI – Load Upper Immediate (add to zero)
  - AUIPC – Add Upper Immediate to PC
Recap: Complete RV32I ISA

RV32I has 47 instructions total
37 instructions covered in CS61C

Not in CS61C

Single-Cycle RISC-V RV32I Datapath

Agenda

- Finish Single-Cycle RISC-V Datapath
- Controller
- Instruction Timing
- Performance Measures
- Introduction to Pipelining
- Pipelined RISC-V Datapath
- And in Conclusion, ...

Processor

Single-Cycle RISC-V RV32I Datapath

Control Logic Truth Table (incomplete)
Control Realization Options

- **ROM**
  - “Read-Only Memory”
  - Regular structure
  - Can be easily reprogrammed
    - fix errors
    - add instructions
  - Popular when designing control logic manually
- **Combinatorial Logic**
  - Today, chip designers use logic synthesis tools to convert truth tables to networks of gates

RV32I, a nine-bit ISA!

![Diagram of ROM-based Control](image)

ROM-based Control

- 11-bit address (inputs)
  - Inst[30,14:12,6:2]
- 9-bit BrEq, BrLT
- 15 data bits (outputs)

ROM Controller Implementation

![Diagram of ROM Controller Implementation](image)

Administrivia

- Homework 2 Due tomorrow 11:59 pm
- Project 1 Part 1 Due Monday Oct. 9
  - Part 2 due Monday Oct. 16
- Midterm 1 Regrades due next Tuesday
  - Talk to a TA if you don’t understand a midterm question or are unsure of a regrade

Break!
Agenda

• Finish Single-Cycle RISC-V Datapath
• Controller
• Instruction Timing
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• And in Conclusion, ...

Instruction Timing

<table>
<thead>
<tr>
<th>Instruction</th>
<th>IF &gt; 200ps</th>
<th>ID &gt; 100ps</th>
<th>ALU &gt; 200ps</th>
<th>MEM &gt; 200ps</th>
<th>WB &gt; 100ps</th>
<th>Total</th>
</tr>
</thead>
<tbody>
<tr>
<td>add</td>
<td>X</td>
<td></td>
<td>X</td>
<td>X</td>
<td></td>
<td>600ps</td>
</tr>
<tr>
<td>iseq</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td></td>
<td>500ps</td>
</tr>
<tr>
<td>sub</td>
<td>X</td>
<td></td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>600ps</td>
</tr>
<tr>
<td>leq</td>
<td>X</td>
<td></td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>500ps</td>
</tr>
<tr>
<td>lw</td>
<td>X</td>
<td></td>
<td>X</td>
<td></td>
<td></td>
<td>500ps</td>
</tr>
<tr>
<td>sw</td>
<td>X</td>
<td></td>
<td>X</td>
<td></td>
<td></td>
<td>500ps</td>
</tr>
</tbody>
</table>

• Maximum clock frequency
  – $f_{\text{max}} = 1/800\text{ps} = 1.25 \text{ GHz}$

• Most blocks idle most of the time
  – E.g. $f_{\text{max,ALU}} = 1/200\text{ps} = 5 \text{ GHz}$
  – How can we keep ALU busy all the time?
  – 5 billion adds/sec, rather than just 1.25 billion?
  – Idea: Factories use three employee shifts - equipment is always busy!

Performance Measures

• “Our” RISC-V executes instructions at 1.25 GHz
  – 1 instruction every 800 ps

• Can we improve its performance?
  – What do we mean with this statement?
  – Not so obvious:
    ▪ Quicker response time, so one job finishes faster?
    ▪ More jobs per unit time (e.g. web server returning pages)?
    ▪ Longer battery life?

Transportation Analogy

<table>
<thead>
<tr>
<th></th>
<th>Sports Car</th>
<th>Bus</th>
</tr>
</thead>
<tbody>
<tr>
<td>Passenger Capacity</td>
<td>2</td>
<td>50</td>
</tr>
<tr>
<td>Travel Speed</td>
<td>200 mph</td>
<td>50 mph</td>
</tr>
<tr>
<td>Gas Mileage</td>
<td>5 mpg</td>
<td>2 mpg</td>
</tr>
</tbody>
</table>

50 Mile trip:

<table>
<thead>
<tr>
<th></th>
<th>Sports Car</th>
<th>Bus</th>
</tr>
</thead>
<tbody>
<tr>
<td>Travel Time</td>
<td>15 min</td>
<td>60 min</td>
</tr>
<tr>
<td>Time for 100 passengers</td>
<td>750 min</td>
<td>120 min</td>
</tr>
<tr>
<td>Gallons per passenger</td>
<td>5 gallons</td>
<td>0.5 gallons</td>
</tr>
</tbody>
</table>
### Computer Analogy

<table>
<thead>
<tr>
<th>Transportation</th>
<th>Computer</th>
</tr>
</thead>
<tbody>
<tr>
<td>Trip Time</td>
<td>Program execution time: e.g. time to update display</td>
</tr>
<tr>
<td>Time for 100 passengers</td>
<td>Throughput: e.g. number of server requests handled per hour</td>
</tr>
<tr>
<td>Gallons per passenger</td>
<td>Energy per task*: e.g. how many movies you can watch per battery charge or energy bill for datacenter</td>
</tr>
</tbody>
</table>

* Note: power is not a good measure, since low-power CPU might run for a long time to complete one task consuming more energy than faster computer running at higher power for a shorter time.

### “Iron Law” of Processor Performance

\[
\text{Time} = \frac{\text{Instructions}}{\text{Cycles}} 
\]

### Instructions per Program

Determined by
- Task
- Algorithm, e.g. \(O(N^2)\) vs \(O(N)\)
- Programming language
- Compiler
- Instruction Set Architecture (ISA)

### (Average) Clock cycles per Instruction

Determined by
- ISA
- Processor implementation (or microarchitecture)
- E.g. for “our” single-cycle RISC-V design, CPI = 1
- Complex instructions (e.g. \texttt{strcpy}), CPI >> 1
- Superscalar processors, CPI < 1 (next lecture)

### Time per Cycle (1/Frequency)

Determined by
- Processor microarchitecture (determines critical path through logic gates)
- Technology (e.g. 14nm versus 28nm)
- Power budget (lower voltages reduce transistor speed)

### Speed Tradeoff Example

For some task (e.g. image compression) ...

<table>
<thead>
<tr>
<th>Processor A</th>
<th>Processor B</th>
</tr>
</thead>
<tbody>
<tr>
<td># Instructions</td>
<td>1 Million</td>
</tr>
<tr>
<td>Average CPI</td>
<td>2.5</td>
</tr>
<tr>
<td>Clock rate</td>
<td>2.5 GHz</td>
</tr>
<tr>
<td>Execution time</td>
<td>1 ms</td>
</tr>
</tbody>
</table>

Processor B is faster for this task, despite executing more instructions and having a lower clock rate!
Energy per Task

\[
\text{Energy per Task} = \frac{\text{Energy} \times \text{Program}}{\text{Program} \times \text{Instruction}} = \frac{\text{Energy}}{\text{Program} \times \text{Instruction}}
\]

“Capacitance” depends on technology, processor features e.g., # of cores

Supplementary voltage, e.g. 1V

Want to reduce capacitance and voltage to reduce energy/task

Energy “Iron Law”

Performance = Power * Energy Efficiency

(Tasks/Second) (Joules/Second) (Tasks/Joule)

- Energy efficiency (e.g., instructions/Joule) is key metric in all computing devices
- For power-constrained systems (e.g., 20MW datacenter), need better energy efficiency to get more performance at same power
- For energy-constrained systems (e.g., 1W phone), need better energy efficiency to prolong battery life

End of Scaling

- In recent years, industry has not been able to reduce supply voltage much, as reducing it further would mean increasing “leakage power” where transistor switches don’t fully turn off (more like dimmer switch than on-off switch)
- Also, size of transistors and hence capacitance, not shrinking as much as before between transistor generations
- Power becomes a growing concern – the “power wall”
- Cost-effective air-cooled chip limit around ~150W

Energy Tradeoff Example

- “Next-generation” processor
  - C (Moore’s Law): -15 %
  - Supply voltage, \( V_{dd} \): -15 %
  - Energy consumption:
    \[ 1 \times (1 - 0.85)^3 = 39 \%
    \]

- Significantly improved energy efficiency thanks to
  - Moore’s Law AND
  - Reduced supply voltage

Processor Trends

Break!
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Pipelining

- A familiar example:
  - Getting a university degree

  ![Year 1](image1)
  ![Year 2](image2)
  ![Year 3](image3)
  ![Year 4](image4)

- Shortage of Computer scientists (your startup is growing):
  - How long does it take to educate 16,000?

Computer Scientist Education

- Option 1: serial
  - 4 years: 4000 enter, 4000 graduate
  - 4 years: 4000 graduate, 4000 graduate
  
- Option 2: pipelining
  - 7 years: 4000 enter, 4000 graduate
  - 4 years: 4000 graduate, 4000 graduate
  - 4 years: 4000 graduate, 4000 graduate
  - 4 years: 4000 graduate, 4000 graduate

  16,000 in 16 years, average throughput is 1000/year

Latency versus Throughput

- Latency
  - Time from entering college to graduation
    - Serial: 4 years
    - Pipelining: 4 years

- Throughput
  - Average number of students graduating each year
    - Serial: 1000
    - Pipelining: 4000

- Pipelining increases throughput (4x in this example)
  - But does nothing to latency
    - Sometimes worse (additional overhead e.g. for shift transition)

Simultaneous versus Sequential

- What happens sequentially?
- What happens simultaneously?
Pipelining with RISC-V

### Timing

<table>
<thead>
<tr>
<th>Phase</th>
<th>Reg Read</th>
<th>ALU</th>
<th>Memory</th>
<th>Reg Write</th>
</tr>
</thead>
<tbody>
<tr>
<td>Instruction Fetch</td>
<td>200 ps</td>
<td>200 ps</td>
<td>200 ps</td>
<td>100 ps</td>
</tr>
<tr>
<td>Reg Read</td>
<td>100 ps</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ALU</td>
<td>200 ps</td>
<td>200 ps</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Memory</td>
<td>200 ps</td>
<td>200 ps</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Reg Write</td>
<td>100 ps</td>
<td>200 ps</td>
<td></td>
<td>200 ps</td>
</tr>
</tbody>
</table>

### Instruction sequence

- add t0, t1, t2
- or t3, t4, t5
- sll t6, t0, t3

### Performance

- Clock rate, \( f \): 1/800 ps = 1.25 GHz
- 1/200 ps = 5 GHz

### Relative speed

1 \times 4 = 4

---

Sequential vs Simultaneous

What happens sequentially, what happens simultaneously?

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### And in Conclusion, ...

- Controller
  - Tells universal datapath how to execute each instruction
- Instruction timing
  - Set by instruction complexity, architecture, technology
  - Pipelining increases clock frequency, "instructions per second"
  - But does not reduce time to complete instruction
- Performance measures
  - Different measures depending on objective
    - Response time
    - Jobs / second
    - Energy per task