University of California at Berkeley
College of Engineering
Department of Electrical Engineering and Computer Science

EECS61C, Spring 2004

HW 07

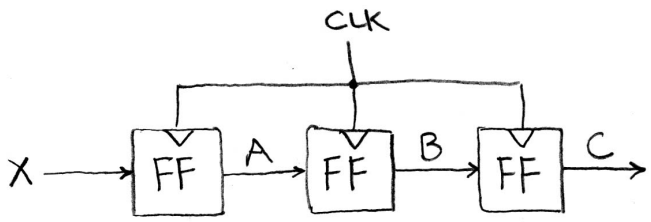
Submitting Your Solution

Submit your solution as hardcopy **before** lecture starts on Friday April 8^{th}. (Submitting it after lecture has started will cost one slip day.) Make sure to clearly mark your paper with your name, login, and section number.

1. Every 18 months to two years a new generation of integrated circuit technology comes out that permits more transistors on a single microprocessor chip. Briefly explain two uses for the extra transistors.

2. The clock signal is guaranteed to be the highest frequency signal in a digital system because it changes twice per clock period (once from low to high, and once from high to low). In a system made of the elements discussed in class (combinational logic blocks and positive edge-triggered flip-flops) what could be the frequency of the next highest frequency signal, in terms of the clock frequency f_{CLK}.

3. Consider the circuit shown below. Assume inputs words, X_0, X_1, ..., arrive one per clock period. Draw the detailed wave for the clock signal and the the signals at point X, A, B, and C in the circuit for four clock cycles. Assume that the clock period is 5ns and the clk-to-q delay is 1ns.

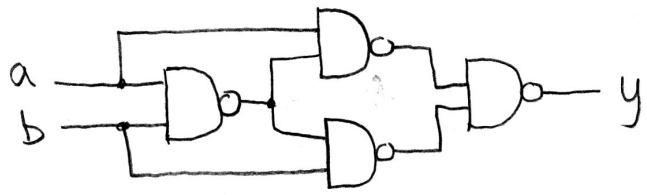


4. Given the accumulator circuit discussed in class and presented in the notes, assume the following: The adder propagation delay is 4ns, the register setup time is 1ns, the register clk-to-q delay is 1ns, and the clock frequency is 200MHz. Will the accumulator function correctly? If not, make two suggestions on how to fix the problem.

5. Design a finite state machine (FSM) with the following behavior. Inputs arrive one bit at a time, one bit per clock cycle. The FSM outputs a 1 if the number of 1's seen at the input thus far is odd and outputs a 0 if the number of 1's seen at the input thus far is even. (You don't need to worry about initialization).

   Do your design in three steps. First draw the state diagram, next specify the truth-table for next state and output based on present state and input, then devise the circuit level implementation.

6. Derive the truth-table for the CL circuit shown below. (Remember, you do this by applying all possible input combination, one at a time). What is the common name of this function?



7. Write the canonical sum-of-products form of a Boolean expression for a 3-input function whose output is a 1 iff the number of 1's in its input is exactly two. (Note: this is not the majority function).

8. Write a simplified Boolean expression for the function represented in the truth-table. *The solution is the OR of two AND terms, each with 2 variables.*

abcd	y
0000	1
0001	1
0010	1
0011	1
0100	0
0101	0
0110	0
0111	0
1000	0
1001	1
1010	0
1011	1
1100	0
1101	1
1110	0
1111	1

9. Using AND gates, OR gates, and inverters, draw a circuit that represents the following Boolean equation:

$$y = \overline{d}(ab + bc)$$

Do no algebraic manipulation.

10. Draw the circuits for a single stage of an adder (one-bit wide adder) using only gates with 2-inputs.