CS61c Spring 2006
Homework 8: Digital Synchronous Designs

Question 1

Without performing any algebraic manipulation, convert the following Boolean expression to a logic gate circuit:

$$z = a(b + c(d + e))$$

Label all inputs and outputs of your circuit.

Question 2

Draw the circuit diagram for the following expression in logic gates assumming no more than 2 inputs per logic gate.

$$y = a + b + c + d + e + f + g + h$$

Try to minimize the delay from inputs to output. Label all your inputs and outputs.

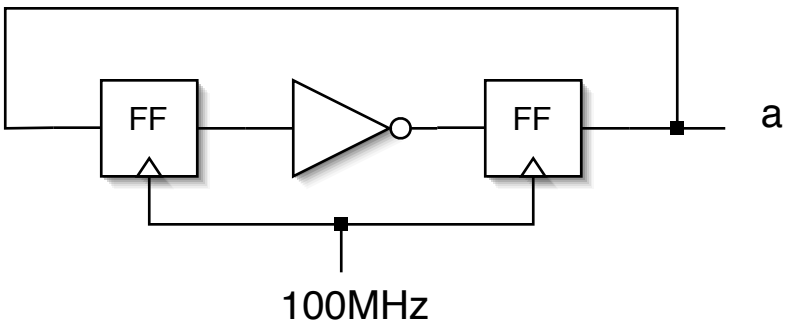
Question 3

Using laws of Boolean algebra and algebraic manipulation, simplify the following expression. Show your steps.

$$abc + a\bar{b}c + ab\bar{c} + a\bar{b}\bar{c}$$

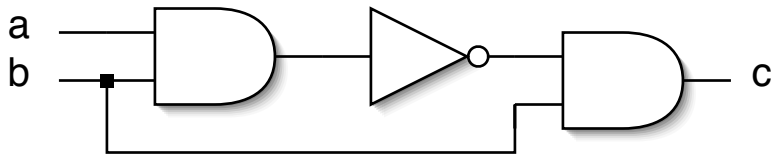
Question 4

Consider the following circuit, at what frequence will the signal a oscillates?



Question 5

Consider the combinational circuit shown below. Each logic gate and inverter have a delay of 1ns.



Assume we apply inputs to the block in the sequence shown below, starting at time 0. Each new input value is applied 1ns after the previous one.

a = 1 1 1 1 1 1 1 1
b = 0 0 0 1 1 1 1 1

The beginning of the output sequence observed at the output `c`, starting at time 0, is shown below. Finish the output sequence that would be observed at the output `c`, by writing down the next four output values that would appear at 1ns intervals.

c = 0 0 0 0 _____ _____ _____ _____

Question 6

Consider the design of a 3-bit unsigned incrementer circuit. It takes as input, the 3-bit number, x_2, x_1, and x_0, and outputs the 3-bit number y_2, y_1, and y_0. The circuit adds 1 to its input. For instance, if the input is 011, the output would be 100. Write the sum-of-products canonical form for y_1, the *middle* bit of the result. *Leave your result in non-simplified form.* Show your steps.

Question 7

Consider the design of a 2-bit wide adder circuit with 2 2-bits inputs a_1a_0 and b_1b_0 that produces a 2-bit output s_1s_0.

Part (a)

Write down the truth table representation for the most significant bit of the output, s_1.

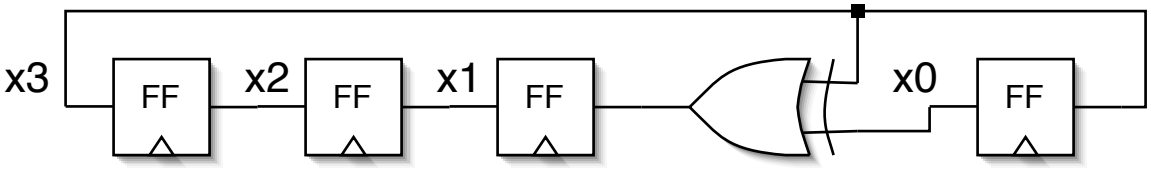
Express the logic function for this bit as a boolean expression in canonical sum-of-product form.

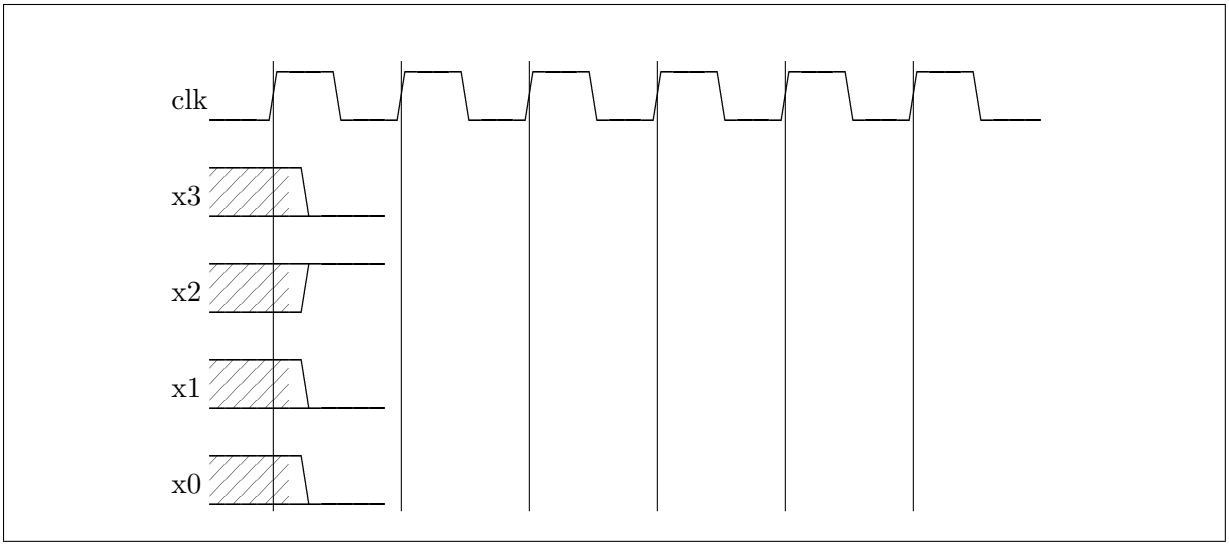
Part (b)

Using the equations derived in lecture for an n-bit adder, express a minimized equation for s_1 in terms of only b_1, b_0, a_1, and a_0.

Question 8

In the following circuit, assume $T_{clk-to-q}$ is 2ns, and the delay of a XOR gate, T_{xor}, is 5ns. All flip-flops (FF) are tied to a 100MHz clock signal which is not drawn for clarity. Initially, $x_3 = 0, x_2 = 1, x_1 = 0$ and $x_0 = 0$. Complete the timing diagram of the first 5 cycles of signal x_3, x_2, x_1 and x_0.





Submission

You should submit your homework electronically using the "submit hw8" command. For questions that require diagram drawings, you may use any graphics drawing programs of your choice, as long as it can produce one of following output format: PDF, PNG, PS, EPS, GIF, JPG.