CS61C Final Review – Problems

1. \texttt{1001 0010 0000 1000 1111 1111 1111 1111}
   a. Interpret this binary string as a two’s compliment integer
   
   b. Interpret this binary string as a floating point number
   
   c. Interpret this binary string as a MIPS instruction

2. How many things can N bits represent?

3. C Problem:

   ```c
   typedef struct node {
   int value;
   struct node* next;
   } ent;

   stack push(stack s, int val) {
   }

   typedef ent* stack;

   int peek(stack s) {
   }

   stack pop(stack s, int* val) {
   }
   ```
4. Implement the push function above in MIPS

Push:

\[
\begin{align*}
\text{li } & \$a0, 8 \\
\text{jal } & \text{malloc} \\
\text{jr } & \$ra
\end{align*}
\]

5. Determine the Boolean expression for \( F \)

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6. How many gates are there for a Boolean function of m inputs and n outputs?

7. Simplify your Boolean expression from 5 using Boolean Algebra

8. Draw the cache and label each access as a hit or miss (and what type of miss)

32 KiB Addressable Memory,
1 KiB Cache Size,
128 B Block Size,
LRU Replacement,
2-way set associative

Memory Accesses:
0x000C
0x10D0
0x2000
0x12D0
0x10D8
0x14D0

9. Indicate the mappings and provide the PPNs for each access:

1 MiB Virtual Memory Space,
32 KiB Physical Memory
4 KiB Page Size

Memory Accesses:
0x0000C
0x200D0
0x10000
0x202D0
0x200D8
0x204D0
10. Give an expression for AMAT of a system with VM (with TLB) and Cache

11. Memory Read – 10%, CPI = 18
   Memory Write – 15%, CPI = 20
   ALU – 30%, CPI = 1
   Branch – 45%, CPI = 2
   Overall CPI?

   CPU Speed = 1 GHz, 1 Million instructions, CPU Time?

   Cache added. Memory Read/Write halved. Improvement?

12. What is the effective speed of a 100 Mbps network that has a 100ms overhead for a transfer of 2 Megabytes.

13. Define and draw each of the Following RAID systems: 0, 1, 4, 5