CISC
COMPLEX INSTRUCTION SET COMPUTER

PERFORMANCE?
DESIGN TIME?
DESIGN ERRORS?
SINGLE CHIP?
PROGRAM SIZE?

RISC
REDUCED INSTRUCTION SET COMPUTER
1970's Design Principles

(1) Semiconductor Memory Growth + Microprogramming
   ⇒ "Costs little for richer instruction sets"
(2) "Move software to "firmware" (microcode)"
   ⇒ Faster & more reliable systems
(3) "Smaller programs are faster programs"
   ⇒ Reduce code size
(4) "Registers are old fashioned" (Hard for compilers)
   ⇒ Memory-to-memory, stacks

"One's eyebrows should rise whenever a future architecture is developed with a register oriented instruction set."

Glenford J. Myers
1978
RISC Design Principles

1. Keep functions simple unless you have a very good reason not to.
   10% increase in cycle time
   \[ \Rightarrow > 10\% \text{ fewer cycles?} \]

2. Microinstructions are same speed as simple instructions.

3. Microcode is not magic.

4. Simple decoding and pipelined execution >> program size

5. Use compiler technology to simplify instructions.
<table>
<thead>
<tr>
<th>Software</th>
<th>Institution</th>
<th>Developer</th>
</tr>
</thead>
<tbody>
<tr>
<td>SCCS</td>
<td>Bell/UCB</td>
<td>Allman</td>
</tr>
<tr>
<td>Mail</td>
<td>UCB</td>
<td>Shoens</td>
</tr>
<tr>
<td>Msgs</td>
<td>UCB</td>
<td>Joy</td>
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<tr>
<td>Caesar</td>
<td>UCB</td>
<td>Ousterhout</td>
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<td>Cifplot</td>
<td>UCB</td>
<td>Fitzpatrick</td>
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<tr>
<td>Mosext</td>
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<tr>
<td>Moserc</td>
<td>Stanford</td>
<td>Baskett</td>
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<td>Powesty</td>
<td>UCB</td>
<td>Cmelik</td>
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<tr>
<td>Moslrc</td>
<td>MIT</td>
<td>Baker</td>
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<tr>
<td>Mossimi</td>
<td>MIT</td>
<td>Terman</td>
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<tr>
<td>Spice</td>
<td>UCB</td>
<td>Pederson</td>
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</tbody>
</table>

RISC

Date 2/17
INSTRUCTION SET RATIONALE FORMATS

GOAL WAS KEEPING SAME SIZE

<table>
<thead>
<tr>
<th>OP</th>
<th>DEST</th>
<th>SOURCE1</th>
<th>SOURCE2</th>
</tr>
</thead>
<tbody>
<tr>
<td>8</td>
<td>5</td>
<td>5</td>
<td>14</td>
</tr>
</tbody>
</table>

32

\[ R_D \leftarrow R_{S1} \quad \text{op} \quad \{ R_{S2} / \text{constant} \} \]

ADD ADDC SHLA SHL AND XOR
SUB SUBC SHRA SHR OR

LOAD(BYTE, WORD, LONG) (SIGNED/UNSIGNED)
STORE(BYTE, WORD, LONG)

\[ R_D \leftarrow M[ R_{S1} + \{ R_{S2} / \text{constant} \} ] \]

CALL RETURN BRANCH

<table>
<thead>
<tr>
<th>OP</th>
<th>DEST</th>
<th>ADDRESS/CONSTANT</th>
</tr>
</thead>
<tbody>
<tr>
<td>8</td>
<td>5</td>
<td>19</td>
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</tbody>
</table>

CALL, RETURN, LOAD IMMEDIATE, BRANCH
PC \leftarrow PC \pm \text{ADDRESS}

NOTE! NO ATTEMPT AT REDUCING CODE SIZE
BUT COULD BE DONE MAKING FETCH MORE COMPLEX
INSTRUCTION FETCH

NORMAL BRANCH | NON-OPT. DELAYED BRANCH | OPTIMIZED DELAYED BRANCH

100  LOAD X,A | LOAD X,A | LOAD X,A

101  ADD I,A | ADD I,A | JUMP 105

102  JUMP 105 | JUMP 106 | ADD I,A

103  ADD B,A, | NO-OP | ADD B,A

104  SUB C,A, | ADD B,A | SUB C,A

105  STORE A,Z | SUB C,A | STORE A,Z

106  STORE A,Z | STORE A,Z
IMPLEMENTATION

3-phase/cycle RISC:

CPU organization

GOLD

Manolis H.G. Katevenis
3 SEP 80

REG. FILE
SH
DATA SH
ALU
DATA IN
PC
INC
3ST
33 pins

BUSSES 32-BITS (ACTUALLY MIXED WITH LOGIC)

CONTROL SIGNALS

Instruction decoder ($q_3$)
RISC-I CPU / OVERLAPPED VERSION / TENTATIVE CHIP PLAN ≈ 5 x 10 mm

19 BONDING PADS + DRIVERS

DECODERS CLOCK BUFFERS

REGISTER FILE

138 x 32

22 x 44 x 3050 x 1400

44 µ x 88 µ x 6.1 mm x 2.8 mm

35 BONDING PADS + DRIVERS

CONTROL

PC's

ALU

OUT- DRIVER

buf. BAR

pre-ch. SHIF.

GRC CROSS

DST

V.C. BERKEU

9 FEB 81
Time for Berkeley to build microcomputer

Industry

4-7 years

$30,000,000.00

100 man years

Experience

U.C. B.

Berkeley Computer Aided Design

Reduced Instruction Set

2 Berkeley Student Years

Beginner’s Luck
<table>
<thead>
<tr>
<th>NAME NO.</th>
<th>SPONSOR</th>
<th>CREW</th>
<th>ENGINE</th>
<th>VAX POWER</th>
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</thead>
<tbody>
<tr>
<td>VAX11 780</td>
<td>DEC</td>
<td>PRO:~30x3yr</td>
<td>'78 Bipolar</td>
<td>1</td>
</tr>
<tr>
<td>MC 68000</td>
<td>MOTOROLA</td>
<td>PRO:~20x3yr</td>
<td>'79 NMOS</td>
<td>1/3</td>
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<tr>
<td>88000</td>
<td>ZILOG</td>
<td>PRO:~15x3yr</td>
<td>'77 NMOS</td>
<td>1/5</td>
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<tr>
<td>8086</td>
<td>INTEL</td>
<td>PRO:~20x2yr</td>
<td>'78 NMOS</td>
<td>1/6</td>
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<tr>
<td>RISC I</td>
<td>U.C.BERK</td>
<td>AM:~10x1yr</td>
<td>'76 NMOS</td>
<td>?</td>
</tr>
</tbody>
</table>

IF BET ONE MONTH SALARY MARCH '80, WHAT FRACTION OF A VAX WOULD BE THE GOAL?
Ave Speed for 11 C programs

VAX-11/780
PDP-11/70
BBN C/70
68000
Z8002
RISC I