Discussion 13: I/O, ECC/Parity, RAID

I/O

1. Fill this table of polling and interrupts.

Operation	Definition	Pro / Good for…	Con / Bad for…
Polling			
Interrupts			

2. Memory Mapped I/O
   Certain memory addresses correspond to registers in I/O devices and not normal memory.
   0xFFFF0000 – Receiver Control:
   Lowest two bits are interrupt enable bit and ready bit.
   0xFFFF0004 – Receiver Data:
   Received data stored at lowest byte.
   0xFFFF0008 – Transmitter Control
   Lowest two bits are interrupt enable bit and ready bit.
   0xFFFF000C – Transmitter Data
   Transmitted data stored at lowest byte.

   Write MIPS code to read a byte from the receiver and immediately send it to the transmitter.

Hamming ECC

Recall the basic structure of a Hamming code. Given bits 1, . . . , m, the bit at position 2^n is parity for all the bits with a 1 in position n. For example, the first bit is chosen such that the sum of all odd-numbered bits is even.

Bit	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Data	P1	P2	D1	P4	D2	D3	D4	P8	D5	D6	D7	D8	D9	D10	D11
P1	X		X		X		X		X		X		X		X
P2		X	X			X	X			X	X			X	X
P4				X	X	X	X					X	X	X	X
P8								X	X	X	X	X	X	X	X

1. How many bits do we need to add to 0011_2 to allow single error correction?

2. Which locations in 0011_2 would parity bits be included?

3. Which bits does each parity bit cover in 0011_2?

4. Write the completed coded representation for 0011_2 to enable single error correction.

5. How can we enable an additional double error detection on top of this?

6. Find the original bits given the following SEC Hamming Code: 0110111_2

7. Find the original bits given the following SEC Hamming Code: 1001000_2

8. Find the original bits given the following SEC Hamming Code: 010011010000110_2

RAID

Fill out the following table:

	Configuration	Pro / Good for…	Con / Bad for…
RAID 0			
RAID 1			
RAID 2			
RAID 3			
RAID 4			
RAID 5			