Problem 1:

Compare the performance of three cache designs for a byte-addressed memory system:

- **Cache 1**: A direct-mapped cache with four blocks, each block holding one word.
- **Cache 2**: A 16B 2-way set associative cache with 4B blocks and LRU replacement policy.
- **Cache 3**: A 16B fully associative cache with 4B blocks and LRU replacement policy.

For the following sequences of memory accesses starting from a cold cache, calculate the miss rate of each cache if the accesses are repeated for a large number of times. All addresses are given in decimal (not hexadecimal).

<table>
<thead>
<tr>
<th>Sequence</th>
<th>Cache 1</th>
<th>Cache 2</th>
<th>Cache 3</th>
</tr>
</thead>
<tbody>
<tr>
<td>a. 0, 4, 0, 4 (repeats)</td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>b. 0, 16, 32, 0, 16, 32 (repeats)</td>
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<td></td>
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<tr>
<td>c. 0, 4, 8, 12, 16, 0, 4, 8, 12, 16 (repeats)</td>
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<td></td>
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<tr>
<td>d. 0, 4, 8, 12, 16, 12, 8, 4, 0, 4, 8, 12, 16, 12, 8, 4 (repeats)</td>
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</tr>
</tbody>
</table>
Problem 2:

**Question 1:**
a. You are given a 16 KiB direct-mapped cache with 128 B blocks and a write-back policy. Assume a 64-bit address space and byte-addressed memory.

Tag: _______  Index: _______  Offset: _______

b. We have a 32-bit byte-addressed machine with an 8-way set-associative cache that uses 32 B blocks and has a total capacity of 8 KiB.

Tag: _______  Index: _______  Offset: _______

**Question 2:**
Look at the following snippet of code.

```
#define LENGTH 16384  // 16384 = 2^14
char A[LENGTH];
for (int i = 0; i < LENGTH; i += 64) A[i] = A[i + 32];  // Loop 1
for (int i = LENGTH / 4; i >= 1; i /= 2) A[i] = A[i * 2];  // Loop 2
```

Let's use the cache parameters given in Part 1a. Assume that A[0] is at the beginning of a cache block and that the cache is initially empty.

a. What is the hit rate of Loop 1? ________________

b. What type(s) of misses occur in Loop 1? ____________________________

c. What is the hit rate of Loop 2? ________________

d. What is the hit rate of Loop 2 if the cache was emptied after Loop 1? ______
Problem 3:

a. Calculate the AMAT for a system with the following properties:
   • L1 cache hits in 1 cycle with local hit rate 20%
   • L2 cache hits in 10 cycles with local hit rate 80%
   • L3 cache hits in 100 cycles with local hit rate 90%
   • Main memory always hits in 1000 cycles

b. How slow can you go? Your system consists of the following:
   • L1 cache hits in 2 cycles with a miss rate of 20%
   • L2 cache hits in 10 cycles
   • Main memory always hits in 300 cycles

You want your AMAT to be <= 22 cycles. What does your local L2 miss rate need to be? What is the equivalent global miss rate?

Problem 4:

a. What is the value of 0xF0000000 if interpreted as a 32-bit floating point number? Recall that the bias for an IEEE 754 32-bit float is 127.

b. What is the smallest number larger than your answer above (Problem 4a) which can be represented by an IEEE 754 32-bit float? Write your answer in hexadecimal.

c. Using IEEE 754 32-bit floating point, what is the largest positive number x that makes this expression true: x + 1.0 = 1.0? Assume that we truncate any bits outside of the significand field. Write your answer in hexadecimal.