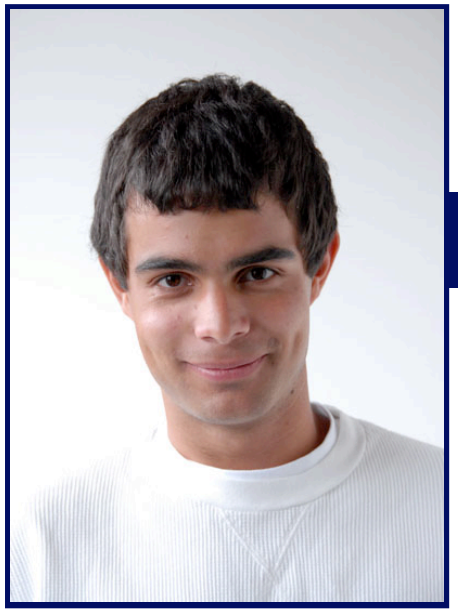
inst.eecs.berkeley.edu/~cs61c

CS61C : Machine Structures

Lecture #31 Summary & Goodbye



2007-8-16

Scott Beamer, Instructor

Cityware Research Project Connects Bluetooth Users on Facebook

Bluetooth™

UNIVERSITY OF BATH

facebook

www.bbc.co.uk

Review

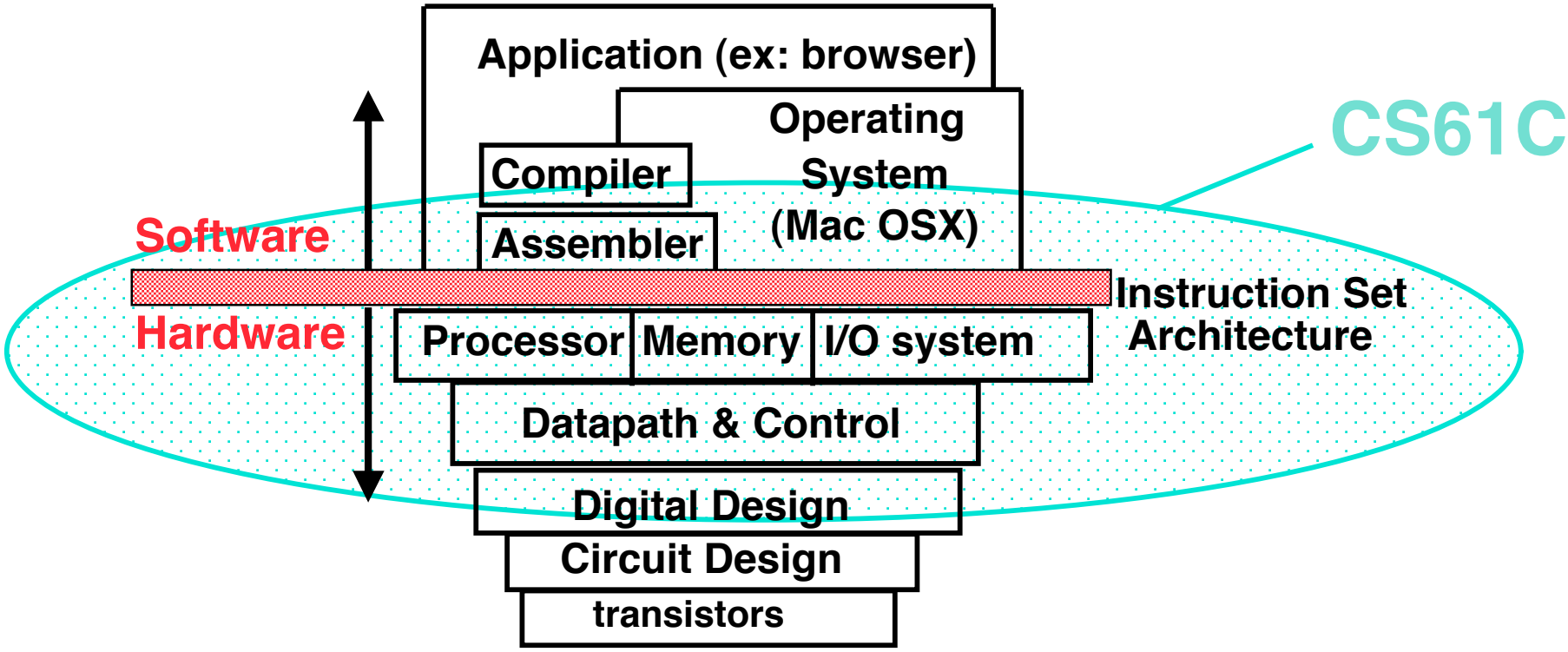
- **Parallelism**
  - Above the line (software, many machines) and below the line (hardware, multiple cores) both critical for computing's future.
  - Hard to write code that fully takes advantage of all available resources to maximize performance and get fully Nx speedup.
  - Distributed and Parallel computing
    - Synchronization hard, APIs help (MapReduce)
  - Hardware Parallelism
    - Cache coherence makes it difficult to scale!
    - Manycore, not multicore!
  - Berkeley EECS taking initative to make ~1000 core HW, put in researchers hands!

CS61C: So what's in it for me? (1st lecture)

Learn some of the big ideas in CS & engineering:

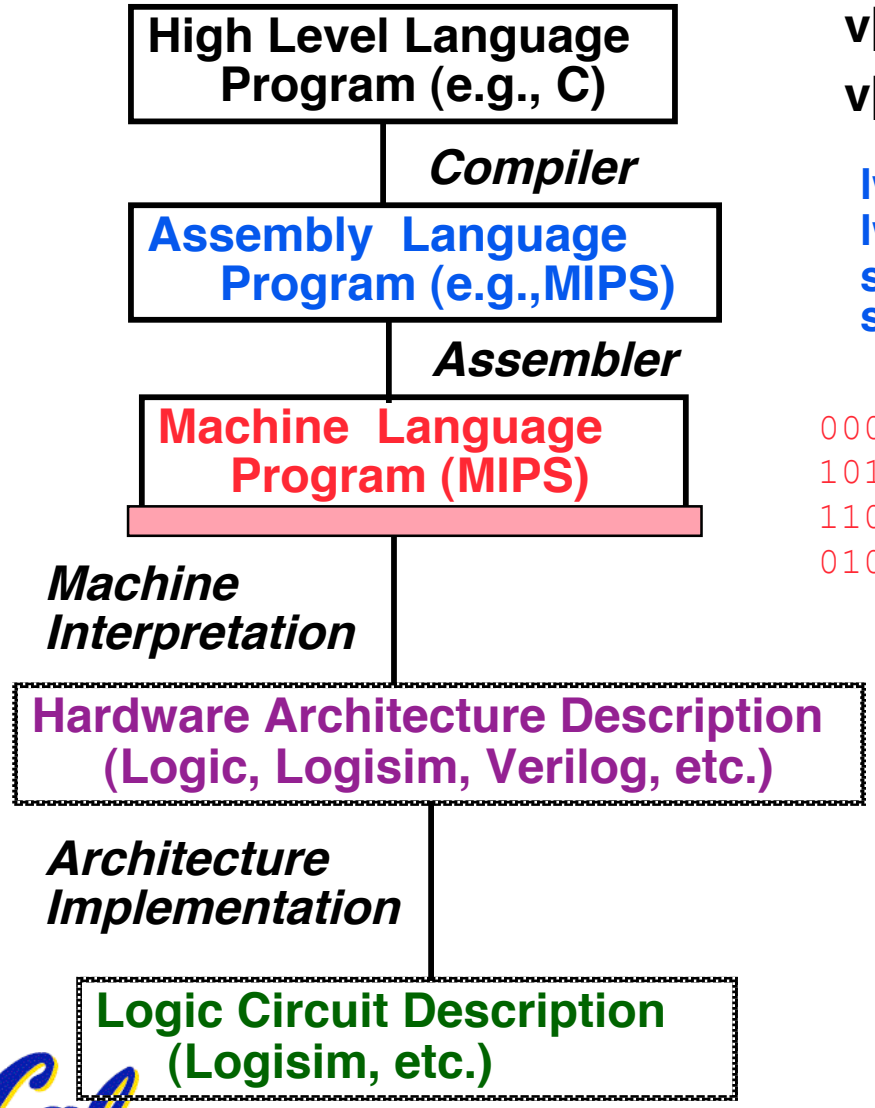
- 5 Classic components of a Computer
- Principle of abstraction, systems built as layers
- Data can be anything (integers, floating point, characters): a program determines what it is
- Stored program concept: instructions just data
- Compilation v. interpretation thru system layers
- Principle of Locality, exploited via a memory hierarchy (cache)
- Greater performance by exploiting parallelism (pipelining, superscalar, MapReduce, multi-..)
- Principles/Pitfalls of Performance Measurement

What are "Machine Structures"?



Coordination of many
levels (layers) of abstraction

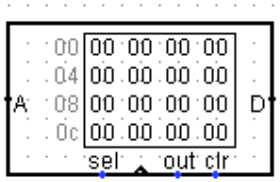
61C Levels of Representation

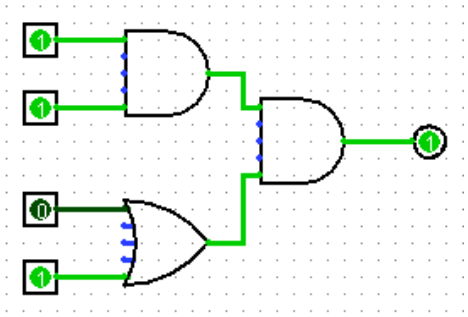



```
temp = v[k];
v[k] = v[k+1];
v[k+1] = temp;
```

```
lw   $t0, 0($2)
lw   $t1, 4($2)
sw   $t1, 0($2)
sw   $t0, 4($2)
```

```
0000 1001 1100 0110 1010 1111 0101 1000
1010 1111 0101 1000 0000 1001 1100 0110
1100 0110 1010 1111 0101 1000 0000 1001
0101 1000 0000 1001 1100 0110 1010 1111
```





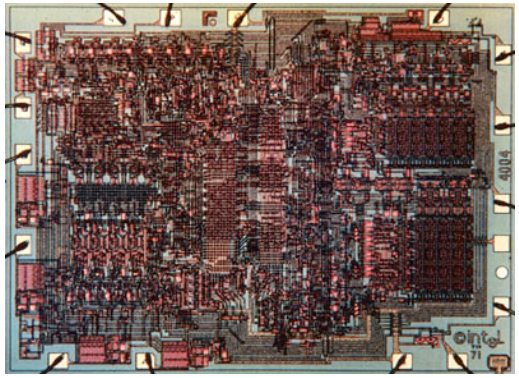
Conventional Wisdom (CW) in Comp Arch

Thanks to Dave Patterson for these

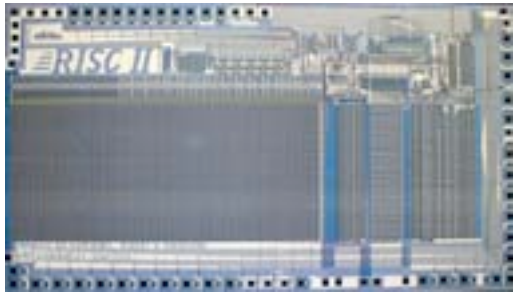
- Old CW: Power free, Transistors expensive
- New CW: Power expensive, Transistors free
  - Can put more on chip than can afford to turn on
- Old CW: Chips reliable internally, errors at pins
- New CW: ≤ 45 nm ⇒ high error rates
- Old CW: CPU manufacturers minds closed
- New CW: Power wall + Memory gap = Brick wall
  - New idea receptive environment
- Old CW: Uniprocessor performance 2X / 1.5 yrs
- New CW: 2X CPUs per socket / ~ 2 to 3 years
  - More simpler processors more power efficient

Massively Parallel Socket

- Processor = new transistor?
  - Does it only help power/cost/performance?
- Intel 4004 (1971): 4-bit processor, 2312 transistors, 0.4 MHz, 10 μm PMOS, 11 mm^2 chip



- RISC II (1983): 32-bit, 5 stage pipeline, 40,760 transistors, 3 MHz, 3 μm NMOS, 60 mm^2 chip
  - 4004 shrinks to ~ 1 mm^2 at 3 micron



- 125 mm^2 chip, 65 nm CMOS = 2312 RISC IIs + Icache + Dcache
  - RISC II shrinks to ~ 0.02 mm^2 at 65 nm
  - Caches via DRAM or 1 transistor SRAM (www.t-ram.com)?
  - Proximity Communication at > 1 TB/s ?
  - Ivan Sutherland @ Sun spending time in Berkeley!

20th vs. 21st Century IT Targets

- 20th Century Measure of Success
  - Performance (peak vs. delivered)
  - Cost (purchase cost vs. ownership cost, power)
- 21st Century Measure of Success? "SPUR"
  - Security
  - Privacy
  - Usability
  - Reliability
- Massive parallelism greater chance (this time) if
  - Measure of success is SPUR vs. only cost-perf
  - Uniprocessor performance improvement decelerates

Other Implications

- Need to revisit chronic unsolved problem
  - Parallel programming!!
- Implications for applications:
  - Computing power >>> CDC6600, Cray XMP (choose your favorite) on an economical die inside your watch, cell phone or PDA
    - On your body health monitoring
    - Google + library of congress on your PDA
- As devices continue to shrink…
  - The need for great HCI critical as ever!

Administrivia

Regrade requests due TODAY at 7

Only for assignments after HW2

Only for grading mistakes

Final Exam

Only bring pen{,cil}s,
two 8.5”x11” handwritten sheets + green.
Leave backpacks, books, calculators, cells & pagers home!
Everyone must take ALL of the final!

Join Us…

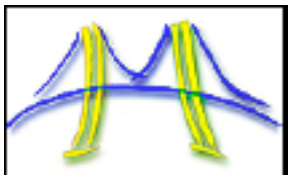
- If you did well in CS3 or 61{A,B,C} (A- or above) and want to be on staff?
  - Usual path: Lab assistant ⇒ Reader ⇒ TA
  - Contact Jenny Jones in 395 Soda before first week of semester for LA signup…
  - Reader/TA forms: `www.cs/~juliea/`
  - I (Dan) strongly encourage anyone who gets an A- or above in the class to follow this path…
    - It will help you internalize the material
    - Help fellow students, (and get paid for it)

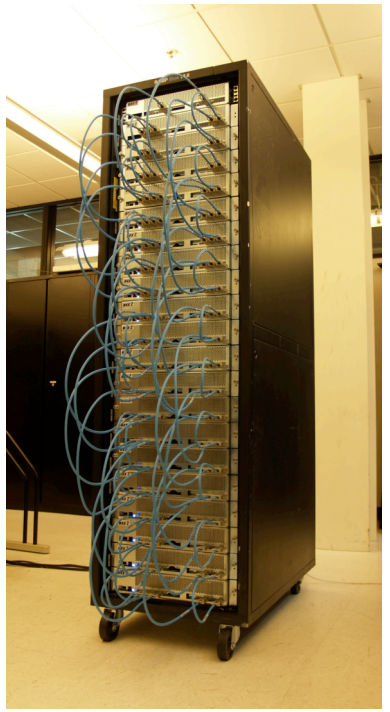
Taking advantage of Cal Opportunities

- **Why are we the #2 Univ in the WORLD?**
  So says the 2004 ranking from the "Times Higher Education Supplement"
  - **Research, reseach, research!**
  - **Whether you want to go to grad school or industry, you need someone to vouch for you! (as is the case with the Mob)**
- **Techniques**
  - **Find out what you like, do lots of web research (read published papers), hit OH of Prof, show enthusiasm & initiative**
- **`research.berkeley.edu/`**
- **`www.eecs.berkeley.edu/Research/`**

Some Current Research

- **RADLab** (Reliable Adaptive Distributed)
  - Looking at datacenter architectures
- **RAMP** (Research Accelerator for Multiple Processors)
  - Use FPGA's to get many cores
  - Picture on right is 1008 cores in 1 rack
- **Berkeley View**
  - Vision for future of parallel





Upper Div's that Build on CS61C

- CS150 - Design Techniques for SDS
- CS152 - Computer Architecture
- CS162 - Operating Systems
- CS164 - Prog. Lang. & Compilers
- CS194-3 - Intro to Computer Systems
- CS198-5 - Networked Computing
- EE122 - Networking

Penultimate slide: Thanks to the staff!

- TAs
  - Valerie Ishida
  - Clark Leung
- Readers
  - Michael Shuh
  - Abhishek Karwa

- Thanks to all the past CS61C Instructors, who have:
  - Trained myself and the staff
  - Made these notes and other course material

The Future for Future Cal Alumni

- What's The Future?
- New Millennium
  - Wireless, Nanotechnology, Quantum Computing, 10 M "volunteer" CPUs, the Parallel revolution...
  - Rapid Changes in Technology
  - World's 2nd Best Education
  - Never Give Up!

"The best way to predict the future is to invent it" – Alan Kay

The Future is up to you!