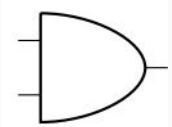
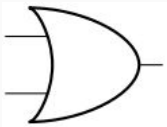
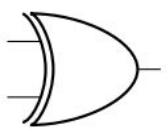
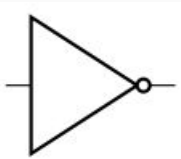
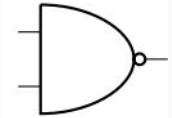
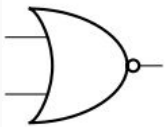
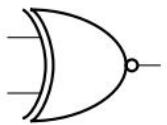
Guerilla Session 3 - Logic & SDS

Connor, Peijie, Sandy

Name:	AND	OR	XOR	NOT
Algebra:	*	+	n/a	! or ———
Gate:				
“Not” Gate:				

Laws of boolean algebra

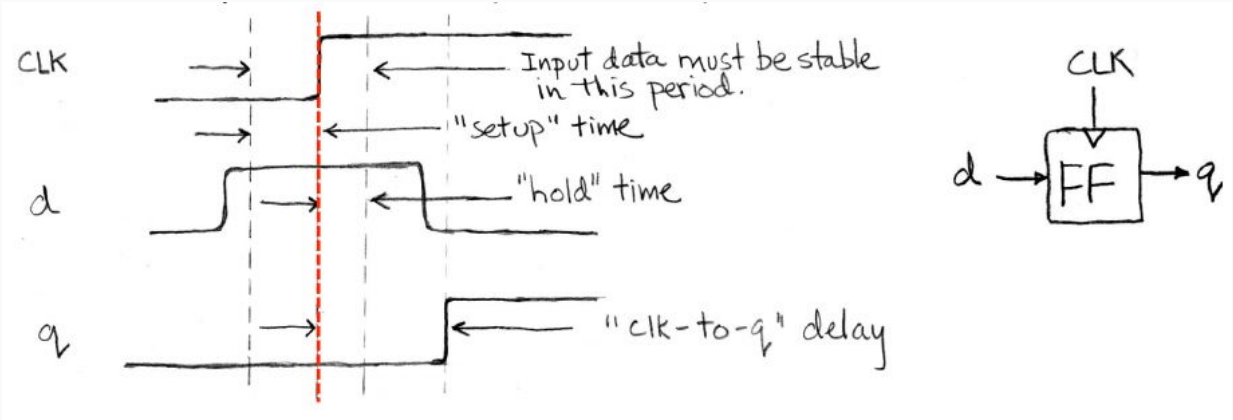
$x \cdot \overline{x} = 0$	$x + \overline{x} = 1$	complementarity
$x \cdot 0 = 0$	$x + 1 = 1$	laws of 0's and 1's
$x \cdot 1 = x$	$x + 0 = x$	identities
$x \cdot x = x$	$x + x = x$	idempotent law
$x \cdot y = y \cdot x$	$x + y = y + x$	commutativity
$(xy)z = x(yz)$	$(x + y) + z = x + (y + z)$	associativity
$x(y + z) = xy + xz$	$x + yz = (x + y)(x + z)$	distribution
$xy + x = x$	$(x + y)x = x$	uniting theorem
$\overline{x}y + x = x + y$	$(\overline{x} + y)x = xy$	uniting theorem v.2
$\overline{x \cdot y} = \overline{x} + \overline{y}$	$\overline{x + y} = \overline{x} \cdot \overline{y}$	DeMorgan's Law

What is a Synchronous System?

- All operations coordinated by a central clock
- Consist of two basic types of circuits, combinational logic and sequential logic
  - Combinational Logic (CL) circuits perform a function on its inputs, e.g. add them and output the result.
  - Sequential Logic (SL) circuits store information, input and output are updated on flip flop of central clock. Used to synchronize flow of information between CL circuits.

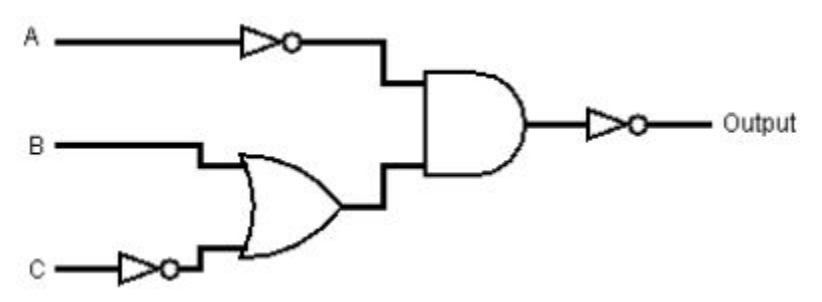
Review of timing terms

- Setup Time: when the input must be stable *before* the edge of the CLK
- Hold Time: when the input must be stable *after* the edge of the CLK
- "CLK-to-Q" Delay: how long it takes the output to change, measured from the edge of the CLK



Critical Path

- The critical path is the path data could flow through in a circuit which would cause the longest delay.
- Max delay = Setup Time + CLK-to-Q Delay + CL Delay
- Assuming we have no registers, and all CL gates have a delay of 10 ns, what's the critical path and max delay of the circuit below?



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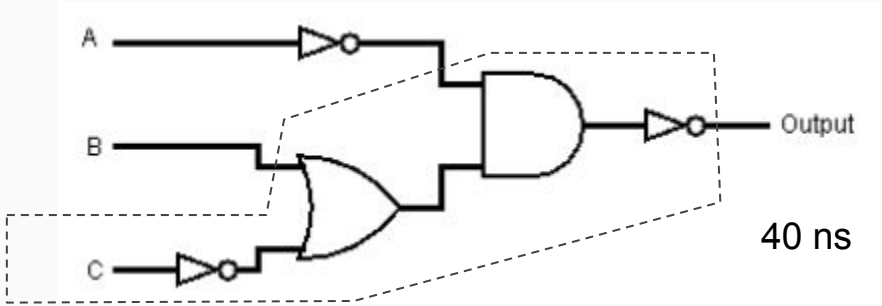

Max Clock Frequency

- When there are registers in the circuit, there are constraints on clock frequency
- Min Period = Max Delay
- Max Freq = 1/Min Period
- Max clock frequency limited by time needed to get correct next state to register (t_setup)
- Two constraints on max clock frequency
  - **t_hold <= t_input <= t_clk_period - t_setup**

Note about Pipelining

- Inserting SL units (registers) between CL Units decreases the length of the critical path, thus allowing the maximum clock frequency to rise and improving data throughput.
- However, more registers means greater latency between the first input and first output

FSM Review

- An abstract machine which can be in one of one of a finite number of states before receiving input and transitioning to another.
- We start at a state and given an input, we follow some edge to another (or the same) state. Possibly outputs as well.
- With combinational logic and registers, any FSM can be implemented in hardware.

FSM example