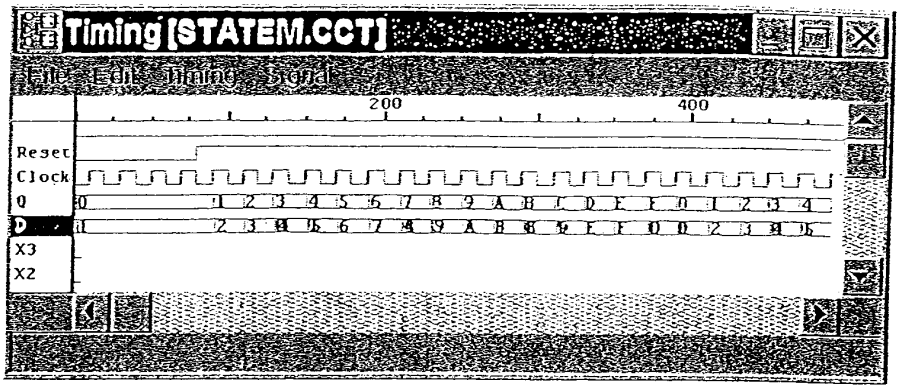
HW 8
Assigned 7 April 2004, due 14 April 2004

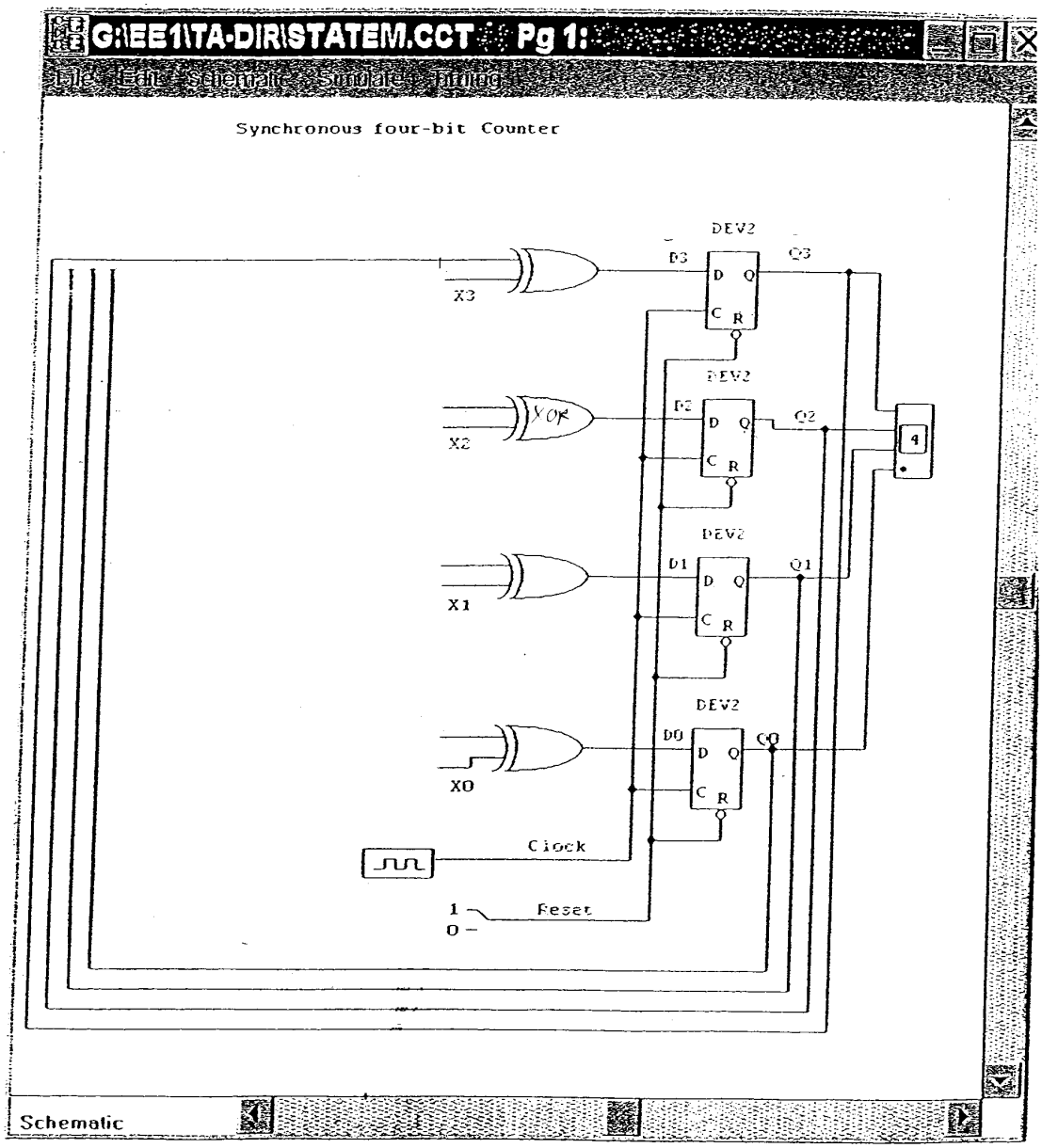
Problem 7.4 – information content of a DNA molecule (10 points).

Problem 22.7. (40 points) Using a program such as LogicWorks™, simulate a synchronous counter, made of interconnected gates and flip-flops, that will count from 0 to 15 clock pulses. Hand in printout of circuit and timing diagram.

Elements of the problem:
1. Synchronous means all latches or flip-flops have a C input to a clock (from DEMOLIB)
2. Output (Qs) advance from 0 decimal to 15 decimal, and then recycle from 0.
3. Output will consist of four bits (the Qs), so you can connect a 4-input hexadecimal display (from DEMOLIB) to show the counter outputs.
4. Use an implementation like (but simpler than!) that for elevator state machine, Fig. 22.12 -- that is, use four D-flip-flops (DEV2 from PRIMGATES) whose respective outputs are the four Qi's. Provide each Di input as the output of an XOR gate, whose two inputs are the respective Qi and another input Xi that is produced by a combinatorial circuit whose inputs can be any of the Qi outputs (this is the feedback).
5. As shown on the layout on opposite side of this page, connect a clock to all of the C inputs, and connect a binary switch (DEMOLIB) to all of the reset (R) inputs to set the counter back to 0.
6. In designing your combinatorial circuit, you should determine what Xi when XORed with Qi will produce the proper value of the data input Di to produce the correct next Qi. You might use the table below to analyze this. (If you want a logical **0** hardwired anywhere, put in a ground from DEMOLIB; if you want a logical **1** hardwired anywhere, put in a +5V supply from DEMOLIB.) Suggestions: write in first the desired values of the Di. Then find the Xi values, starting with X0, the easiest. Write out the truth table for an XOR gate to help keep it in mind. Focus on the places where the D values change from **0** to **1**. Simplify your circuits for X2 and X3 by using boolean algebra.

q 3	q 2	q 1	q 0	d 3	d 2	d 1	d 0	x 3	x 2	x 1	x 0
0	0	0	0								
0	0	0	1								
0	0	1	0								
0	0	1	1								
0	1	0	0								
0	1	0	1								
0	1	1	0								
0	1	1	1								
1	0	0	0								
1	0	0	1								
1	0	1	0								
1	0	1	1								
1	1	0	0								
1	1	0	1								
1	1	1	0								
1	1	1	1								


Timing [STATEM.CCT]
File Edit Timing Signal
200
400
Reset
Clock
Q
D
X3
X2


G:\EE1\TA-DIR\STATEM.CCT Pg 1:
File Edit Schematic Simulate Timing
Synchronous four-bit Counter
DEV2
D3
Q3
X3
D2
Q2
X2
XOR
4
D1
Q1
X1
D0
Q0
X0
D
Q
C
R
Clock
1
0
Reset
Schematic